

# Syndicated

News, tips, and notes for improving the Quality of Results in FPGA and ASIC design

## Quick Partitioning Technology

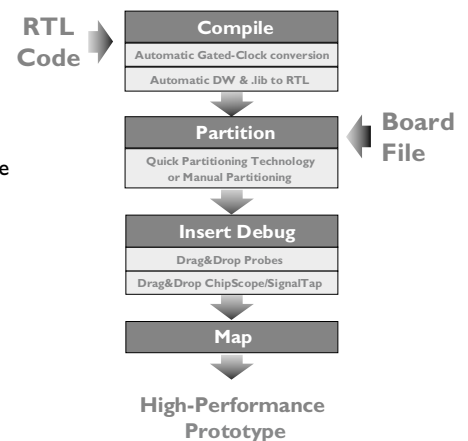
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**Quick** Partitioning Technology (QPT) is a new automatic RTL partitioning capability introduced in Certify® 5.0 software. QPT provides benefits to both experienced prototype designers and those new to prototyping. To understand the technology and benefits, let's first review the prototyping methodology and process.

### Prototyping Methodology

Prototyping is a methodology for implementing an ASIC design into a single FPGA or multiple FPGA hardware in order to validate the functionality at near real-time speeds. To understanding QPT and its benefits, we'll focus on the multiple FPGA flow addressed by the Certify tool. This diagram shows the prototyping design flow. In this flow, a design is compiled from RTL. If present in the design, ASIC gated-clock structures are converted to clock enables and translation of non-RTL components, such as Designware elements and instantiated gates, is done. After compiling, the design is then partitioned either by manual partitioning, QPT, or a combination of the two. Often when a prototype is running, it is necessary to observe signals internal to the FPGAs, so debug logic is inserted to enable this. Certify software supports probes, multiplexed probes, Xilinx ChipScope, and Altera SignalTap to allow internal debug access. Once the design is partitioned and any debug logic added, it can be mapped to the target FPGAs and the prototype completed.

As seen in this flow, partitioning is a key element of prototyping. In the past, the Certify tool has provided partitioning help as a guided interactive process. This enables a designer to manually assign design elements to a particular FPGA via drag-and-drop or the Impact Analysis UI. The designer is given immediate graphical feedback on their assignments and how it affects I/O usage, area usage, and design module interconnects. For engineers familiar with prototyping and its complexities, this has been a good solution. But for companies who have not used prototyping in the past, or new design engineers not familiar with the methodology, partitioning is an unfamiliar process requiring trial and error. QPT provides a solution to this.



### Flexible Partitioning Technology

QPT is the first automatic RTL partitioning technology. This provides tremendous ease of use and speed for the designer. Once the design compiled, the designer can choose to use QPT via a simple menu selection. The designer can also optionally set target goals for I/O and area usage for each FPGA. If no user targets are set, QPT uses the default setting of 100% I/O utilization and 80% area utilization. QPT is then run via a single menu selection. The performance of QPT is very fast. One example, a 600K gate design partitioned on a Pentium III computer in 44 seconds. Another 2 million-gate design was partitioned in less than two minutes using QPT. Aside from the time saving benefits of this level of performance, the speed of QPT allows designers to try "what if" analysis of different board configurations for a design. With manual partitioning, the effort to redo partitioning on different board configurations was enough effort that most projects would just settle on a large enough board for the design. With QPT, a designer can, within minutes, try different board configurations to get a board with just enough capacity in order to reduce cost or target a board for whatever goal is desired.

In addition to the speed and ease of use, QPT also delivers excellent Quality of Results. Interestingly, QPT has delivered comparable results in I/O and area utilization to an experienced ASIC designer familiar with the design and the prototyping process. This allows a designer not familiar with the design or with prototyping methods to get results via QPT that would normally require an experienced senior designer. Companies already using prototyping methodologies can

now use less experienced designers to complete the prototypes, while companies not yet using prototyping can adopt the methodology more easily.

QPT is also very flexible. A design can be partitioned with QPT only, manual partitioning then QPT, or QPT followed by manual partitioning changes. Most designers will likely want to use only QPT, but there are some examples where a combination is beneficial. For those requiring maximum performance from a prototype, time-critical parts can be partitioned manually to insure that performance is met. QPT can then be run and the remaining design elements will be automatically partitioned. For those designs where performance is not critical but minimizing hardware is, QPT can be run on a design with a smaller than normally required hardware board. QPT will deliver the best results it can, but will usually run out of I/Os first (as would a designer). After QPT has finished, the designer can then manually apply CPM (Certify Pin Multiplexing to time-share I/O pins) to reduce the number of needed I/Os. This will result in less performance, but will allow a design to fit in a smaller hardware device than normally required.

Certify 5.0 software is the first production version with Quick Partitioning Technology. In this first implementation, there are a few restrictions to using QPT. Those are:

- Black boxes must be manually assigned.
- Flattened boards are required; hierarchical boards are not yet supported.
- CPM must be manually performed if required.
- Traces are ignored on pre-defined boards.

Future versions of the Certify product with QPT will address these restrictions.

For more information on the incorporation of QPT in the Certify solution, you can go to [www.synplicity.com/products/certify.html](http://www.synplicity.com/products/certify.html) or call your local sales representative directly. ☎