

# The Syndicated®

A Technical Newsletter for ASIC and FPGA Designers

## Corporate Tips & Hints

### Synplify Pro® Software

**Q.** What is the Actel \_SDC.SDC file?

**A.** The \_SDC.SDC file is a file used to communicate design constraints from the Synplify Pro product to Actel's Designer software.

Starting with version 8.0, Synplify Pro software writes out the \_SDC.SDC file along with the EDIF netlist during synthesis to be used as input to the Actel Designer tool. Since the Synplify Pro tool already uses the file extension .SDC for the Synplify Pro input timing constraint file, we use the \_SDC.SDC name to distinguish the Synplify Pro generated output design constraint file for Actel.

The current \_SDC.SDC statements the Synplify Pro and Actel Designer tools support are:

Synplify Pro Constraint File	Actel Constraint File
Define_clock	create_clock
Define_path_delay	set_max_delay
Define_multicycle_path	set_multicycle path
Define_false path	set_false_path
Define_input_delay	set_input_delay
Define_output_delay	set_output_delay

The translation from Synplify Pro timing constraints to Actel design constraints are transparent to the end user. Once the \_SDC.SDC and EDIF files are generated by the Synplify Pro software, the user simply imports both files into Actel's Designer version 6.2 or later software and proceeds using the normal backend tool flow.

### Amplify FPGA® Software


**Q.** How do I guarantee that logic assigned to a physical region remains inside the region?

**A.** The Amplify FPGA product enables you to create physical regions on an FPGA and then assign RTL to those regions. These physical constraints are used during physical synthesis to perform simultaneous placement and logic optimizations. A common optimization is one that tunnels (moves) sequential logic from one physical region to another; however in some cases you may not want this behavior. For these situations, Amplify FPGA software provides an option that may be assigned to a region that disables sequential tunneling. To disable sequential tunneling on a region, select the region, click the right mouse button to view the region menu, and select "Tunneling → Disable". Disabling tunneling on the region guarantees that all RTL assigned to the region remains inside the region.

### Identify® Software

**Q.** Can I debug my mixed language design using Identify software?

**A.** The Identify 2.2 product release specifically addresses mixed language designs. While previous versions of Identify software only allowed instrumentation in the top-level language, this latest release can compile all levels of a mixed language design and allow instrumentation in all sections of the design. As with the Synplify Pro solution, identify 2.2 software requires that the top-level entity/module be explicitly set in the GUI or imported from a Synplify Pro software PRJ file.

With Identify 2.2 software, you can continue instrumenting and debugging HDL across language barriers in your design. The Identify product will automatically produce instrumentation in the correct language and account for bus encoding and VHDL enumerations. 



Simply Better Results

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