

## ASIC Solutions

### Simplify 90-nm Design with NEC Electronics' ISSP90 Family of Structured ASICs

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The ongoing migration of custom ICs to smaller, more advanced process geometries has shown that the performance requirements of today's electronic products continue to rise. This presents a challenge to the majority of ASIC designers working with advanced process technologies like 90-nm, as market and economic pressures require them to develop high-performance chips under tight time-to-market and NRE cost constraints. These pressures are in direct conflict with the characteristics of 90-nm ASIC implementation. The mask, development time, and NRE costs associated with 90-nm development can be quite high. With the majority of custom chips developed today only reaching small- to medium-sized production runs (5,000 - 100,000 units), achieving a return on investment for the development of a 90-nm ASIC has become increasingly difficult.

To bridge the gap between market needs, performance needs, and economic and engineering realities, NEC Electronics has developed the Instant Silicon Solution Platform™ (ISSP™) of structured ASIC devices. The ISSP90 family is designed to serve the needs of customers requiring performance similar to that of a 90-nm cell-based ASIC. Based on NEC Electronics' 90-nm UX6 CMOS process technology, highly integrated, low-power ASIC in a significantly shorter development time and at a fraction of the cost traditionally associated with cell-based ASICs.

#### High-Performing, Rapidly Customizable Silicon

NEC Electronics' ISSP90 structured ASICs use a seven metal-layer interconnection structure consisting of five fixed layers and two customizable layers. The logic architecture is made up of complex multi-gates for implementing custom logic or synthesizable IP functions. The two customizable layers are where designers configure the ISSP90 device to support their specific application.

Below the two customizable layers, pre-verified design-for-test (DFT) circuits, clocktrees, and power lines are immersed into three fixed metal layers which also serve as interconnect to embedded IP cores. An additional fixed metal mask layer on top of the customizable layers is used to reinforce the power lines. The final fixed mask layer is used to support FCBGA packaging. By using the ISSP90 architecture's fixed and customizable layers, designers are essentially building a device that offers performance and density levels very similar to a cell-based ASIC in a fabric that accelerates design and manufacturing turnaround time.

The ISSP90 devices are ideal for supporting complex systems that designers typically implement when working at 90-nm. The ISSP90 family offers two masterslice types: one optimized for high-density applications, and one optimized for high-speed applications. There are multiple gate, memory, and I/O configurations available. ISSP90 structured ASICs offer designers up to 6.5M usable ASIC gates, 5.7M Mbits of configurable embedded SRAM, and clock speeds of up to 500MHz. The various specifications of the masterslices in the ISSP90 family are described in greater detail in Table 1.

Master	Usable Gates	Embedded SRAM	RAM#	PLL#	Master DLL	Slave DLL	I/O Interface	Package FCBGA	Signal Count
<b>High-Density Masters</b>									
μPD69551	1.74M	1.11 Mb	60	8	2	14	3.3V	1155/729	520
μPD69552	2.68M	1.92 Mb	104	8	2	20	3.3V	1155/729	660
μPD69553	3.45M	2.95 Mb	160	8	2	26	3.3V	1521/1155	800
μPD69554	4.00M	1.77 Mb	96	8	2	26	3.3V	1521/1155	800
μPD69555	4.67M	4.20 Mb	228	8	2	32	3.3V	1521/1155	940
μPD69556	5.53M	2.36 Mb	128	8	2	32	3.3V	1521/1155	940
μPD69557	5.40M	5.68 Mb	308	8	2	38	3.3V	1849/1521	~1024
μPD69558	6.50M	3.02 Mb	164	8	2	38	3.3V	1849/1521	~1024
<b>High-Speed Masters</b>									
μPD69561	0.87M	0.77 Mb	42	8	2	14	3.3V	1155/729	520
μPD69562	1.34M	1.34 Mb	73	8	2	20	3.3V	1155/729	660
μPD69563	1.73M	2.06 Mb	112	8	2	26	3.3V	1521/1155	800
μPD69564	2.00M	1.24 Mb	67	8	2	26	3.3V	1521/1155	800
μPD69565	2.34M	2.94 Mb	160	8	2	32	3.3V	1521/1155	940
μPD69566	2.76M	1.65 Mb	90	8	2	32	3.3V	1521/1155	940
μPD69567	2.70M	3.97 Mb	216	8	2	38	3.3V	1849/1521	~1024
μPD69568	3.25M	2.12 Mb	115	8	2	38	3.3V	1849/1521	~1024

Table 1: Specifications for ISSP90 masterslices

#### Fast, Economical Design with Low Risk

Most importantly, designers using the ISSP platform can build a high-performance structures ASIC with a much shorter development cycle and at a lower overall NRE cost than a traditional standard cell-based ASIC. The majority of this design advantage is attributable to the pre-embedded features in the ISSP90 architecture's lower metal layers. The pre-embedded power grid and clock domains simplify resolution of power and signal integrity issues, and accelerate timing closure. And since these base layers are pre-configured with a variety of popular testing methodologies, designers do not have to spend time adding DFT circuits to their design and going through lengthy design iterations. Compared to the 12 to 18 months required to develop and manufacture a typical cell-based ASIC, designers using an ISSP90 structured ASIC can accelerate their development time and receive engineering samples in four to six months. Specific features of the ISSP90 architecture that help reduce design time are listed in Table 2.

Feature	Benefit
Embedded clock structure	Assures predictable and minimized clock skew
Embedded power mesh	Results in fewer power integrity issues
Embedded DFT features	Requires no test insertion, no functional/timing resimulation
Precharacterized IP	Allows designers to concentrate on product design

Table 2: Fast design turnaround times

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**“Simplify 90-nm” continued from page 1**

These features translate into lower development costs than required to design a cell-based ASIC. Fewer mask steps and easier resolution of signal integrity, power integrity, and timing closer issues result in fewer engineering hours, lower tooling costs, and lower NRE costs. While a typical five-million-gate cell-based ASIC design implemented in 90-nm can require an upfront NRE cost of anywhere from \$1M to \$3M and the purchase of six to ten EDA tools costing more than \$300K, designers using a comparable ISSP90 device can spend less than \$200K in NRE and need only two to three tools costing less than \$50K to develop their product.

Additionally, NEC Electronics helps eliminate design risk and increases the likelihood of first-pass silicon by offering a highly optimized design flow that helps resolve many of the traditional back-end design issues that have threatened the success of high-density cell-based ASIC designs. By partnering with Synplicity®, NEC Electronics offers designers a physical synthesis design tool, Amplify® ISSP physical synthesis, that is specifically optimized for ISSP90 structured ASICs.

Amplify ISSP software features embedded knowledge of the ISSP90 architecture. With a detailed understanding of the architecture’s embedded complex multi-gate, clocktree, and power grid during synthesis, the Amplify ISSP product allows engineers to quickly achieve timing closure and avoid the highly iterative process that typical characterizes ASIC design. Working off a detailed floorplan, the Amplify ISSP tool maps directly to the ISSP architecture, resulting in a more optimized implementation and a more predictable result. While a generic physical synthesis tool in a cell-based ASIC design can estimate only about 40 percent of all the routes in a design, the Amplify ISSP product, with its embedded knowledge of the architecture, can estimate up to 70 percent of all routes. Designers gain better utilization, faster timing closure, and fewer design iterations, resulting in a shorter time to tapeout.

90-nm for the Masses

The dramatic time and cost savings provided by NEC Electronics’ ISSP90 family of structured ASICs brings the performance advantage of 90-nm custom silicon to a much broader group of designers, who will in turn deliver high-performance ASIC solutions to the OEMs building tomorrow’s products. For more information about design benefits ISSP90 structures ASICs can bring to your 90-nm product development plans, visit NEC Electronics America at

[www.necelam.com/issp](http://www.necelam.com/issp). ■



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