

Tips & Hints

Synplify® DSP

Q. Can I expand the Synplify DSP blockset?

A. Yes, Synplify DSP includes the capability for designers to add their own IP to the Synplify DSP blockset. We call this a “Custom Blockset” and it is very easy to do. A designer simply creates a Simulink library and enters the functionality they desire in a Simulink Subsystem, just like you would normally do during algorithm development using the Synplify DSP blockset as the design elements. The next step is to create a “mask”. This is a Simulink concept that essentially helps you to create an icon for your block AND to make it optionally parameterizable. Finally, put your library in your MathWorks search path. It can then be reused in any design with the full benefits of the Synplify DSP system level optimizations. For detailed instructions, see “Creating Customer Blocksets” in the Synplify DSP User Guide.

Synplify Pro® Software

Q. How do I control what logic goes into the DSP48 elements in the new Virtex-4 FPGA from Xilinx?

A. Synplify Pro software has the ability to place common DSP structures, such as multipliers and multadds, within the DSP48. However, if you find that the configuration that the Synplify Pro software uses is not the one you want for your design, you can control the DSP48s with the `syn_dspstyle` attribute that has been added for Synplify Pro software version 7.7.

This attribute can take a value of either “logic” or “dsp48” and you simply attach it to the sections of your code that you want to control. For example, if you have several multipliers in your design, but there are not enough DSP48s on your FPGA to fit them in, the Synplify Pro software, based on density and timing, will select which ones go in the DSP48s. If, however, you want more control, you can use the attribute as follows:

```
module test(a,b,clk,p);
input [9:0] a,b;
input clk;
output [19:0] p;

reg [19:0] p;
wire [19:0] mult /* synthesis syn_dspstyle = "logic" */;

assign mult = a * b;

always@(posedge clk)
    p <= mult;

endmodule
```

Amplify® FPGA Physical Synthesis Software

Q. What are the differences between using *groups* in the Synplify® product and creating *physical regions* in the Amplify product?


A. Area groups specified on modules in the Synplify Pro product are used in the Compile Point flow to support the Xilinx Incremental flow. This information is forward annotated to the Xilinx place-and-route tool. The Synplify Pro product does not use the area-group information to influence synthesis. Unlike the Synplify Pro solution, when you create a physical region in the Amplify tool and assign RTL instances to this region, the Amplify tool uses this information during synthesis to perform optimization and produces an optimized gate-level netlist. Another point to note is that the Amplify tool creates a new physical hierarchy for this region. The area groups on this region are used to inform the Xilinx place-and-route tool where to place the new physical hierarchy.

Identify® RTL Debugger

Q. How do I instrument my current Synplify software project for debugging using the Identify Instrumentor?

A. Beginning with Synplify software version 7.7, there is a new icon in the toolbar for launching the Identify Instrumentor. This button provides a more integrated flow between the two tools by launching the Identify Instrumentor with the data from your current Synplify project already loaded.

When clicked, this button launches the Identify Instrumentor, or alternately allows you to locate a specific Identify software installation for execution. Once launched, the Identify solution imports the current Synplify project, including design files, toplevel unit, and device family.

From the Identify Instrumentor, you can select signals and breakpoints for instrumentation and configure the debug logic for your particular situation. After saving this instrumentation, you can then synthesize and place-and-route the instrumented design and begin debugging your design. 



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