

## ASIC Solutions

### **Structured ASIC Platforms with Integrated SERDES Cores Deliver Excellent Performance with Low-Cost**

*by Simone Shaghafi, ASIC Marketing Manager, Fujitsu Microelectronics America, Inc.*

**Integrated** structured ASIC platforms with serialization/deserialization (SERDES) technology have set a new performance standard for applications that require wide bandwidth capability. Many industry analysts now suggest that by 2007 a majority of custom designs will use SERDES technology to increase system bandwidth and reduce overall system costs.

But integrating SERDES cores into a structured ASIC platform is not a trivial task. When selecting a multigigabit platform with integrated SERDES, it is very important to select a field-proven platform and work with a vendor who has the practical expertise to solve challenging design issues.

#### **Why SERDES?**

When upgrading existing equipment, designers are required to stay within the same physical space while improving bandwidth and speed in their applications. SERDES technology addresses the critical issues that alleviate the I/O bottleneck. The technology compresses slower-speed parallel data into much faster serial data. For example, in a networking application, the serializer in the SERDES block converts 400 MHz parallel data coming from inside the network card to 3.125 Gbps serial data as output to the backplane bus. The deserializer in another SERDES block then retrieves the serial data from the bus and converts it back to slower parallel data. By implementing these techniques, the net traffic flowing across the line-card-to-backplane interface is increased by a factor of two to four times that of the incoming data rate.

Utilizing SERDES technology also results in reduced pin counts needed to carry a given data bandwidth. In the case of 16-bit parallel data, the pin count reduction is factor of 8 (differential pair). So, by implementing SERDES technology, it is possible to increase the maximum data bandwidth through the available connector pins at the backplane interface.

In addition, integrating SERDES also means lower system-level power consumption and lower cost because fewer external components and fewer parallel wires are needed to route at the board level.

#### **AccelArray Provides Proven, Tested SERDES Integration**

When selecting a platform ASIC vendor, customer must consider a range of SERDES specifications, such as low jitter performance, low power, and noise resistance. But the most critical issue is the vendor's knowledge of signal integrity issues achieved at the circuit level. The ability to drive signals over a long FR4 distance is a critical factor. The platform ASIC vendor must have the knowledge and expertise to analyze signal integrity and other system design issues to ensure low risk and first time success.

Fujitsu's AccelArray technology offers a proven, fully verified and tested platform with integrated SERDES functionality that reduces the total ASIC pin count dramatically leading to smaller and lower cost chips. For example, by using SERDES, it is possible to replace 16 I/O pins with just two I/O pins (differential pair) per SERDES channel. In a structured ASIC platform with 24 channels, instead of 384 I/O pins, only 48 pins are needed.

Fujitsu has pioneered the development of high-speed SERDES used in integrated ASICs running at high-speed systems design, and has demonstrated silicon with 64 channels of 3.125G SERDES. In building AccelArray platforms, Fujitsu applied more than a decade of expertise and experience developing complex ASIC designs for applications such as networking and storage networking.

As part of the AccelArray technology, Fujitsu has also developed new low-risk, proven Giga platforms with 16 and 24 channels of embedded SERDES, operating at up to 3.125Gbps, with total aggregated BW of up to 150Gbps fully duplexed. The platforms use a universal SERDES solution that supports multiple standards such as XAUI, PCI Express, Serial Rapid I/O, and Fibre Channel. They support up to 3Mb of true dual port SRAMs, with more than five million raw logic gates.

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Also, Fujitsu can demonstrate that its embedded SERDES ASIC can tolerate the losses that can occur with multi-gigabit traffic over PCB traces, and also with XAUI system backplane circuit boards and backplane connectors.

Using the AccelArray Giga platform to implement SERDES provides real benefits in terms of cost and performance, while guaranteeing the time to market advantages of structured ASICs and reducing the risk of delays. 



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Synplicity, Inc.  
600 W. California Avenue  
Sunnyvale, CA 94086 USA  
Phone: (US) +1 408 215-6000  
Fax: (US) +1 408 222-0263  
[www.synplicity.com](http://www.synplicity.com)

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