

SYNOPSYS®

Predictable Success

“Some of the bugs that come up in real life today require that we monitor a thousand signals or more at the same time. Thanks to the Identify tool, we're able to tackle and fix these complex bugs.”

— Sandesh Bharadwaj,
Staff Engineer,
MIPS Technologies



Synplicity®

Simply Better Results

Success with the Synopsys Synplicity® Business Group and MIPS

Identify® RTL Debugger Success Story

Introduction

For MIPS Technologies, one of the world's leading providers of processor IP, debugging is a critical element in the design of its industry-standard processor cores. In 2006, MIPS Technologies began using the Identify RTL debugging product from Synopsys' Synplicity Business Group in the validation flow, and quickly achieved success with a particularly challenging class of bugs. Debugging a class of problems with the Identify tool has proven to be extremely fast, simple and effective.

In its first few months in MIPS's arsenal, the Identify solution helped speed the completion of two key designs by allowing the engineering team to quickly find several bugs that threatened processor performance.

MIPS Encounters Bugs that Defy Emulators and Logic Analyzers

MIPS Technologies is a leading provider of industry-standard processor architectures and cores for digital consumer, networking, personal entertainment, communications and business applications. MIPS Technologies licenses its intellectual property (IP) to today's leading semiconductor companies, ASIC developers and system OEMs, who benefit from reduced costs and development cycles as well as accelerated time-to-market.

Microprocessor designs are highly complex and difficult to debug. It is crucial to employ the fastest, easiest-to-use environments for debugging and verifying these designs. MIPS Technologies has used both emulators and logic analyzers to identify and fix a variety of bugs, but there were drawbacks. The emulator was excruciatingly slow - 25 times slower than an FPGA. Bugs that arose once a day on an FPGA, for example, could easily take 25 days to resolve using the emulator, time that the debugging schedule did not permit. For intermittent bugs that arose only every few hours or days, MIPS employed logic analyzers but found that process time-consuming and tedious, and pin limitations imposed severe restrictions on the number of signals that could be monitored at once.

In early 2006, MIPS engineers encountered a problem while validating a new system that resisted resolution with both methods. The problem arose infrequently, rendering the emulation approach too time-consuming. But diagnosing the problem required monitoring a great many signals, far more than they could hook up to a logic analyzer at once, and by the time the team determined which signal to monitor, it was too late to see the behavior that caused the bug. They simply had to find another solution.

Identify RTL Debugger Success Story

Identify RTL Debugger Combines Speed, Ease of Setup, and the Power to Pinpoint Difficult Bugs

“What we needed was a way to quickly probe all the signals of interest without making any hardware modifications at all,” said Sandesh Bharadwaj, Staff Engineer for MIPS. “Fortunately we were already working closely with Synplicity because we use the Synplify Pro[®] tool for FPGA synthesis, and we learned about the Identify tool. It appeared to be just the solution we were looking for - and we weren't disappointed.”

Synplicity installed the Identify solution on an evaluation basis and MIPS quickly converted it to a purchase for two reasons: The product lived up to expectations, and Synplicity complemented it with outstanding support. “Synplicity was very helpful during the ramp up time,” reported Bharadwaj. “They were always quick and provided informed answers to our questions. Therefore, we were up and running with the Identify product in no time.”

The first problem that MIPS' engineers addressed with the Identify software was to find and fix the bug that had caused them to find a better solution, which proved to be straightforward. They were able

to quickly set up probes on signals that promised to help diagnose the problem, recompile, and run their tests. Through this process, MIPS quickly identified the source of the problem, fixed it, and verified the solution. Later, the Identify software helped pinpoint another difficult bug on the same design, helping the company speed the product to market. Then, MIPS commenced debugging the next product in line and found the Identify software to be invaluable for locating yet another elusive bug.

“The Identify solution allows us to probe signals at the RTL level so that we don't have to concern ourselves with gate-level netlists,” said Bharadwaj. “It contains very powerful mechanisms for setting up triggers, in essence allowing us to set up state machines to do the triggering. So to use it to debug a problem, all we have to do is establish probes to dump all the signals of interest, set up triggers, do a recompile, and start up our tests. Right away we're watching waveforms that let us zero in on the problem.”

To learn more about the Identify product, visit <http://www.synplicity.com/products/identify>.

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Synopsys, Inc.
Synplicity Business Group
600 West California Avenue
Sunnyvale, CA 94086 USA
www.synplicity.com