

TotalRecall™ Full Visibility Technology - Frequently Asked Questions



General

What is TotalRecall?

TotalRecall is Synplicity's new full visibility verification technology that enables ASIC or FPGA designers to find and fix functional bugs using FPGA hardware.

What does TotalRecall technology do?

TotalRecall technology allows ASIC and FPGA designers to capture the full state (all register & memory contents) of a live, running FPGA at a specified number of clock cycles before a trigger event occurs. In addition, TotalRecall automatically creates the testbench that may be used in a standard HDL simulator to recreate the error event as often as necessary to identify the error.

What types of users or applications will benefit from TotalRecall technology?

TotalRecall technology is especially useful for FPGA-based ASIC prototyping because it accelerates testing to FPGA hardware speeds then automatically provides a detailed testbench for debug in an HDL simulator. This method is significantly faster than using an HDL simulator.

High-end FPGA designs will also benefit from TotalRecall technology because of the time saved during the verification phase of the design.

What are the main benefits of TotalRecall technology?

TotalRecall technology benefits design verification because it:

- Brings the visibility of errors within FPGA-based ASIC prototypes up to the level of an HDL simulator
- Dramatically reduces the time required to verify ASIC prototypes or large FPGA designs
- Captures the full state of a design leading up to the point where an error condition occurs and transfers the state and an automatically generated testbench to an HDL simulator for further analysis
- Allows assertions synthesized into the FPGA hardware to be used as triggers. Also allows complex trigger conditions such as FSMs. TotalRecall technology enables designers to trigger on anything from simple signal values or code branches, such as CASE and IF statements, to complex combinations of signals and branches. Complex sequential state machines to be used as precision trigger controls can also be created.
- Can be used with popular HDL simulators

When will products containing the TotalRecall technology be available?

Synplicity is in development on a product containing TotalRecall technology. Beta testing with customers will begin in early 2007

How much will products containing TotalRecall technology cost?

Pricing information will be available when products containing the TotalRecall technology are announced.

TotalRecall Technology Details

How can synthesized assertions be used?

The synthesized assertion logic may be used in two ways:

1. to capture the design state at a user-defined point prior to the assertion trigger and transfer it to an HDL simulator along with the testbench that lead up to the assertion trigger
2. to keep running past the initial failure and log all the assertion failures that occur in a file for reporting and analysis later

What assertions does TotalRecall technology support?

In the initial release, OVL (Open Verification Library) will be supported. Support for SVA and PSL assertions are planned for future releases.

What size designs can TotalRecall technology be applied to?

- There is no pre-defined size limit to which TotalRecall technology can be applied.
- TotalRecall technology requires additional on-chip logic area which can be controlled by the user

Does the FPGA board configuration need to be changed to accommodate the TotalRecall technology?

No, as long as the FPGA being deployed has sufficient capacity. An alternative would be to use a larger FPGA with the same package and pinout.. When the debug is completed a designer may simply revert back to the smaller capacity part.

Does TotalRecall technology capture the memory contents?

Yes. It can capture the memory contents for RAM, FIFOs, Shift Registers, etc. Debugging memory content is one of the most tedious and time consuming process. The technology captures and transfers memory state at a user-defined point prior to a trigger condition and transfers it to an HDL simulator along with the testbench that lead up to the trigger.

Can TotalRecall technology be used on more than just a single module within a design?

Yes. The entire design contained within an FPGA may be used with TotalRecall technology. This enables the user to get a complete understanding of design behavior in context of the rest of system components.

Are there patents issued on TotalRecall technology?

Yes, there has been one patent issued and others pending on this technology.



Synplicity, Inc.
600 W. California Ave, Sunnyvale, CA 94086
Phone: (408) 215-6000, Fax: (408) 222-0264
www.synplicity.com

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