



SRAM_1x1

SRAM Daughter Board



Part of the Confirma™ ASIC/ASSP Verification Platform

SRAM_1x1 contains a synchronous SRAM subsystem. Memory sizes of 144 to 288 Mbits are available, with a 72-bit wide data bus. Standard memory size is 2Mx72 bits pipelined.

Features

- Form factor: 1x1 (occupies one daughter board connector)
- Mounted with 4 JEDEC standard ZBT, FT, pipelined or other versions of synchronous SRAM devices
- Standard board rated at 133 MHz
- Input clock is sent back to the motherboard through the dedicated clock pin (A60)
- "Top side" connectors allows up to 5 SRAM_1x1 to be stacked
- Runs on 3.3V powered HAPS system (some configurations will work with 2.5V as well)

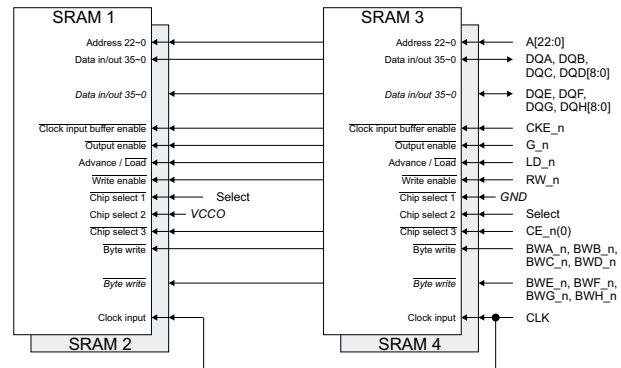
Clocks

The SRAM clock is generated on the motherboard and the clock is fed back through the dedicated clock input of the motherboard connector as a phase reference.

Modes

The SRAMs can be configured for pipeline or flow through mode operation. Burst sequences can be configured for linear or interleaved operation.

Block Schematic



Stacking SRAM_1x1

Up to 5 SRAM_1x1 boards can be stacked on top of each other. The board select signals are routed to the corresponding chip select signals via the top side connectors as shown below.

