DesignWare Library

DW8051 MacroCell

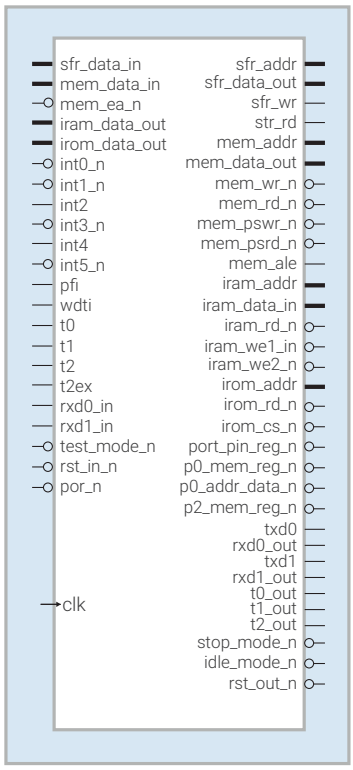
Highlights

- High-performance, configurable, fully synthesizable 8051 core
- Binary compatible with industry standard 803x/805x microcontrollers
- Technology-independent
- ASIC and FPGA technologies
- Easy to use
- Includes coreConsultant™ tool

Overview

The DesignWare® DW8051™ MacroCell is a high-performance, configurable, fully synthesizable 8051 core that is binary compatible with the industry standard 803x/805x microcontrollers. The DW8051 core is technology-independent and has been fabricated in both ASIC and FPGA technologies. Designed for ease of use, the DW8051 includes the coreConsultant™ tool, a user-friendly wizard, which guides users through configuration, simulation and synthesis.

The DesignWare DW8051 MacroCell solution includes the DW8051 MacroCell, a reference design, and Synopsys' extensive verification environment. The high-performance architecture of the DW8051 provides up to three times performance improvement over the standard 8051 when operating at the same clock rate.



DW8051 Input/Output Signals

Proven Quality, Complete Solution

To ensure quality, the DW8051 was developed according to Synopsys' strict design-for-reuse methodology. It has undergone extensive testing during the design process and has been proven in many different technologies. It has also been tested with a variety of third-party 8051 development tools and 8051 evaluation boards.

The DW8051's high-performance, config-urable, synthesizable architecture, combined with the development environment, provides a total solution for building low-cost, high-performance embedded control systems for a wide range of applications.

Automated Design Flow with Synopsys coreConsultant

The DW8051 MacroCell solution includes the Synopsys coreConsultant tool, which provides the following services:

- Activity checklist that guides users through DW8051 design activities in the correct order
- Automatic, error-free DW8051 configuration, including parameter cross-dependency checking
- Automatic configuration and operation of the DW8051 verification environment
- Automatic, high-quality synthesis with users' technology library and installed version of Design Compiler™
- Automatic design checking and synthesis results analysis

Users can operate coreConsultant in its GUI mode (Figure 1) or in batch mode through its command line interface.

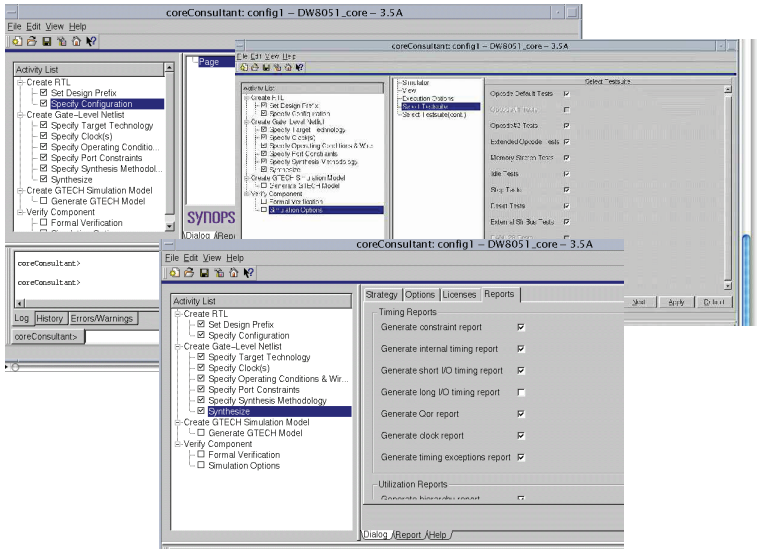


Figure 1. Example coreConsultant dialogs for DW8051

Technical Advantages of the DW8051

- 4 clocks/instruction cycle versus 12 in standard 8051: up to three times faster execution on average versus standard 8051
- Stretch memory cycle
  - Allows application software to adjust to different external RAM speeds
  - MOVX in as little as eight clock cycles
- Dual data pointers
  - Improves efficiency when moving large blocks of data
- Internal/external peripheral interface
  - Special function register (SFR) bus in DW8051 supports both internal and external peripherals vs. internal only in standard 8051
- Two optional full-duplex serial ports
- Seven additional interrupts
- SFR bus for adding custom peripherals

803x/805x Compatibility

The DW8051 is compatible with the standard 8051 instruction set and can be configured to a wide range of industry standard 803x/805x architectures. Control signals for standard 803x/805x I/O ports are included. Optional full-duplex serial ports and third timer are selectable through parameters.

High-Performance Architecture

The DW8051 is a fully static and synchronous design. Eliminating wasted bus cycles and providing dual data pointers for moving large data blocks achieve greater efficiency and performance. The DW8051 MacroCell typically contains ~10k-13k gates, depending on the configuration and technology in which it is implemented. It runs at greater than 300 megahertz in 90-nm process technology. Lower performance applications also benefit by being able to run at lower clock rates to get the same performance as a standard 12 clocks/instruction 8051. Lower clock rates lead to lower power consumption and lower electro-magnetic interference (EMI).

Adding Custom Designed Peripherals

A typical 8051 allows peripheral interface only through port logic. In addition to the ports, the DW8051 also provides direct access to peripherals through the memory and SFR buses (Figure 2).

- Users can interface additional peripherals directly to the DW8051's memory bus. This method allows them to make use of the "stretch" memory cycle feature to interface slow peripherals.
- Users can also directly attach custom designed peripherals to the efficient SFR bus, the same bus used for interfacing the standard DW8051 internal peripherals. SFR addresses that are not used for the DW8051 internal SFRs are available for connecting external peripherals. Adding peripherals to the SFR bus offers the following advantages:
  - Faster read, write accesses; 1 clock vs. 2 clocks using mem_bus
  - Direct addressing
  - Takes advantage of bit manipulation instructions
  - Efficient, compact code

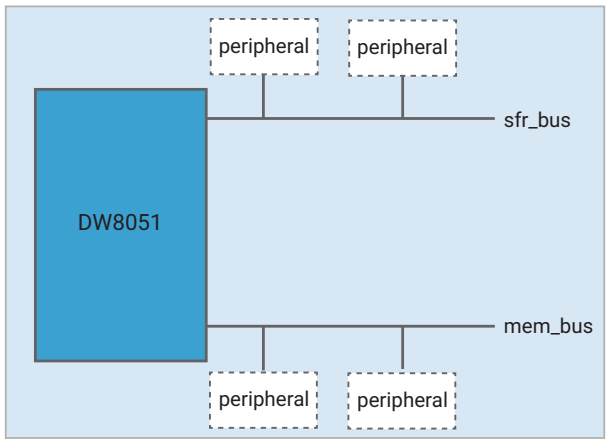


Figure 2. DW8051 external SFR and memory bus

Third-Party Development Tools Support

Synopsys has an active program in place to support third-party tools. Many industry standard compilers, assemblers, ROM monitors, and in-circuit emulators have been tested for compatibility with the DW8051. This allows integration of these tools into a design environment and provides a complete development solution for DW8051-based embedded systems on a chip. Nohau Corporation and Hitex Development Tools provide in-circuit emulation support.

DW8051 Configurable Architecture

Figure 3 illustrates the hardware architecture of the DW8051 core. The name of the top-level module is DW8051_core. The internal RAM and ROM modules are located outside DW8051_core to facilitate simulation and insertion of technology-specific RAM/ROM modules. The following sub-modules and interfaces are selectable through parameter settings:

- DW8051_core can address either 128 or 256 bytes of internal RAM
- The internal ROM address range is deter-mined by a parameter (rom_addr_size)
- Timer 2 (DW8051_timer2) is optional
- 0,1, or 2 serial ports (DW8051_serial) can be implemented
- The interrupt unit is either DW8051_intr_0 (6-source) or DW8051_intr_1 (13-source)

The coreConsultant tool automatically generates the selected DW8051 configuration so that no HDL source code editing is needed.

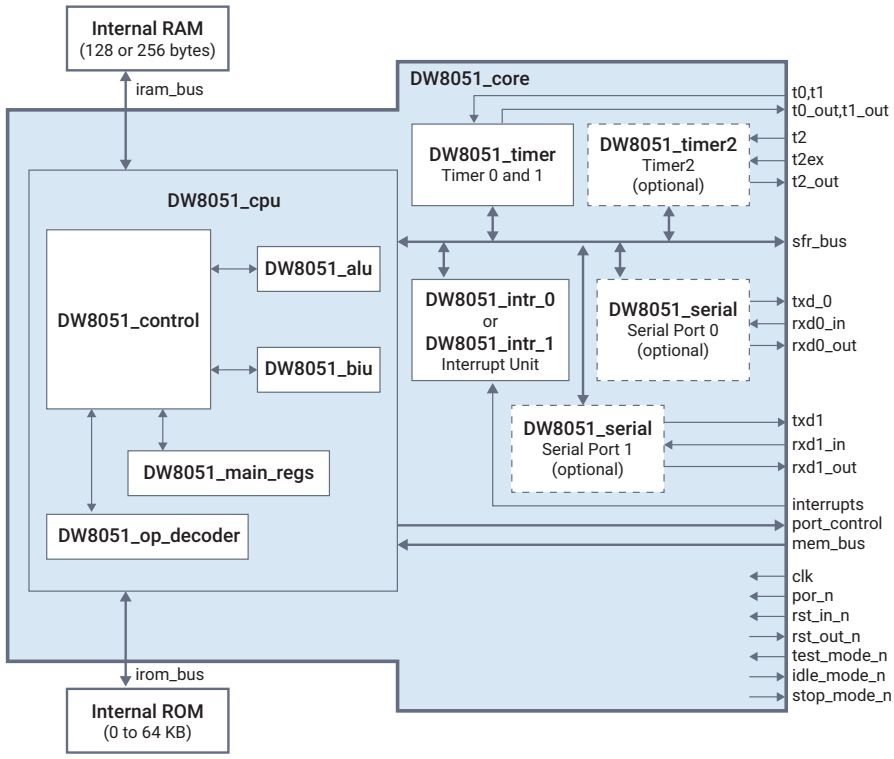


Figure 3. DW8051_core

803X/805X Feature Comparison

Through parameter settings, user scan configure the DW8051 hardware to be functionally compatible with a variety of 803x/805x configurations. For example, users can implement two 16-bit timers for compatibility with the Intel 8051, or they can implement three 16-bit timers for compatibility with the Intel 80C32 (Table 1).

Feature	Intel				Dallas DS80C320	DesignWare DW8051
	8031	8051	80C32	80C52		
Clocks Per Instruction Cycle	12	12	12	12	4	4
Internal ROM (1)	—	4KB	—	8KB	—	Up to 64KB
Internal RAM (1)	128 bytes	128 bytes	256 bytes	256 bytes	256 bytes	128 bytes or 256 bytes
Data Pointers	1	1	1	1	2	2
Serial Ports	1	1	1	1	2	0,1, or 2
16-bit Timers	2	2	3	3	3	2 or 3
Interrupt Sources (total of int. and ext.)	5	5	6	6	13	6 or 13
Stretch Memory Cycle	No	No	No	No	Yes	Yes

(1) Internal ROM and RAM are located outside of DW8051_core.

Table 1. Feature summary of DW8051 and common 803x/805x configurations

Performance Overview

The DW8051 processor core offers increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051 (Figure 4). The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

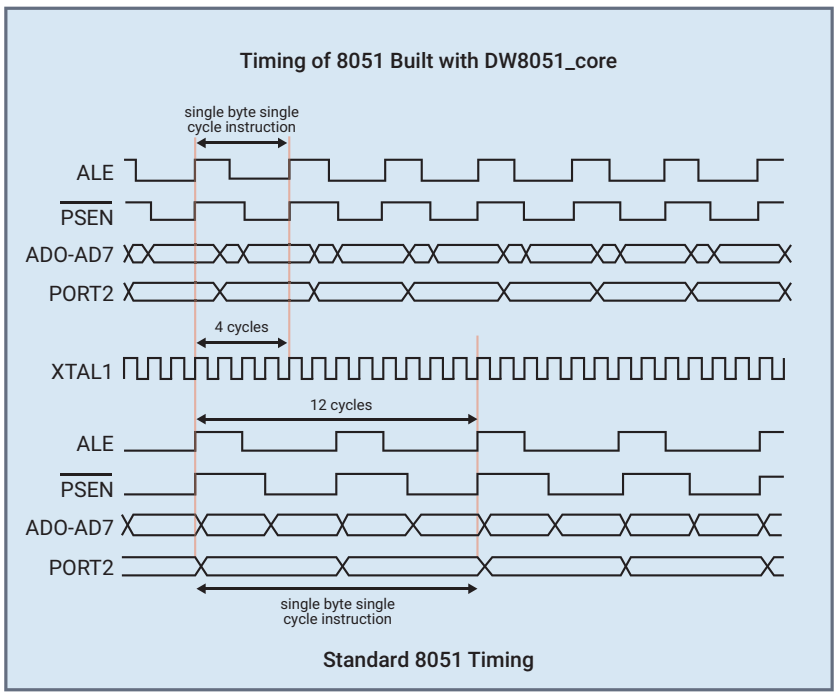


Figure 4. Instruction cycle timing comparison

Some instructions require a different number of instruction cycles on the DW8051 than the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the DW8051 architecture, instructions can take between one and five instruction cycles to complete. The average speed improvement for the entire instruction set is approximately two-and-a-half times (Table 2).

Number of Opcodes	Speed Improvement
150	3.0X
51	1.5X
43	2.0X
2	2.4X

Note: Comparison is for DW8051 and standard 8051 operating at the same clock frequency.

Table 2. Performance comparison of DW8051 vs. Standard 8051

DW8051 Development Environment

The DW8051 MacroCell solution is devel-oped and packaged for use with Synopsys' coreConsultant tool. The complete DW8051 MacroCell solution coreKit includes:

- The DW8051 MacroCell
- Multiple-simulator support (e.g., VCS, MTI ModelSim, Verilog-XL and NC-Verilog)
- An example 8032-compatible design: this design uses the DW8051_core and illustrates how to build and connect 8051-compatible port modules for designs where it is preferable to use standard 8051 port modules instead of the 16-bit address memory interface
- Extensive verification environment
  - HDL testbench that instantiates the DW8051_core, models internal ROM and RAM, and emulates 64-kilobytes of external RAM and 64-kilobytes of external ROM
  - Processes that trace the program counter and write accesses to external RAM
  - A collection of 8051 assembler programs that test all of the instruction set opcodes, plus miscellaneous tests for internal hardware
  - A set of expected results (golden log files)
  - Automatic testbench configuration, simulation, and results checking through coreConsultant
- Example scan insertion script for Synopsys DFT Compiler™
- Example TSMC .18µm Library
- Complete documentation: DW8051 data book in on-line format (PDF), integrated into the coreConsultant on-line help
- Support for third-party development tools
  - Industry standard compilers, assemblers, debuggers, ROM monitors, in-circuit emulators from Nohau and Hitex
  - Keil 8051 software development tools
- Comprehensive worldwide technical support

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

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