

Benefits of Signoff Tools in Physical Design

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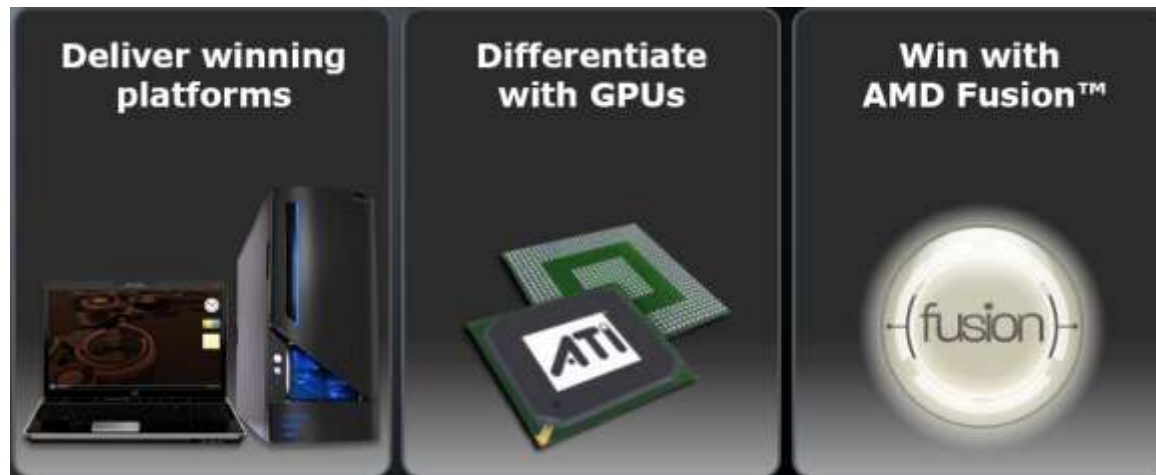
Member of Technical Staff / GPU CAD

Design Automation Conference
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About AMD

- An innovative technology company designing industry-leading
 - x86 microprocessors
 - Chipsets
 - Graphics, video, and multimedia products and technologies
- AMD product strategy



Technology and Architecture of a GPU

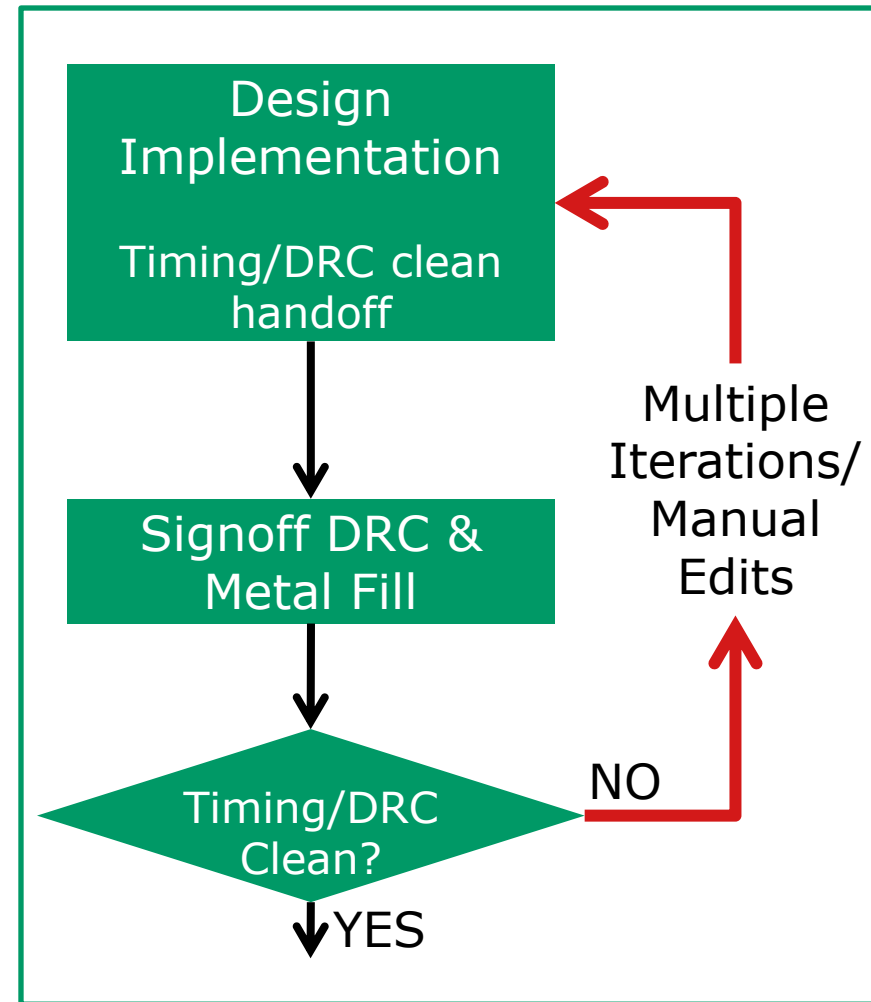
- TSMC 40nm technology
- 9 metal layers
- 71 unique ASIC blocks
- IO macros are full custom designed
- 380mm² die area with 2.15 billion transistors

- 1,600 stream processors
- 1.2GHz GDDR5 memory
- 4.8GHz data memory throughput
- 2.7 TFLOPS in single precision



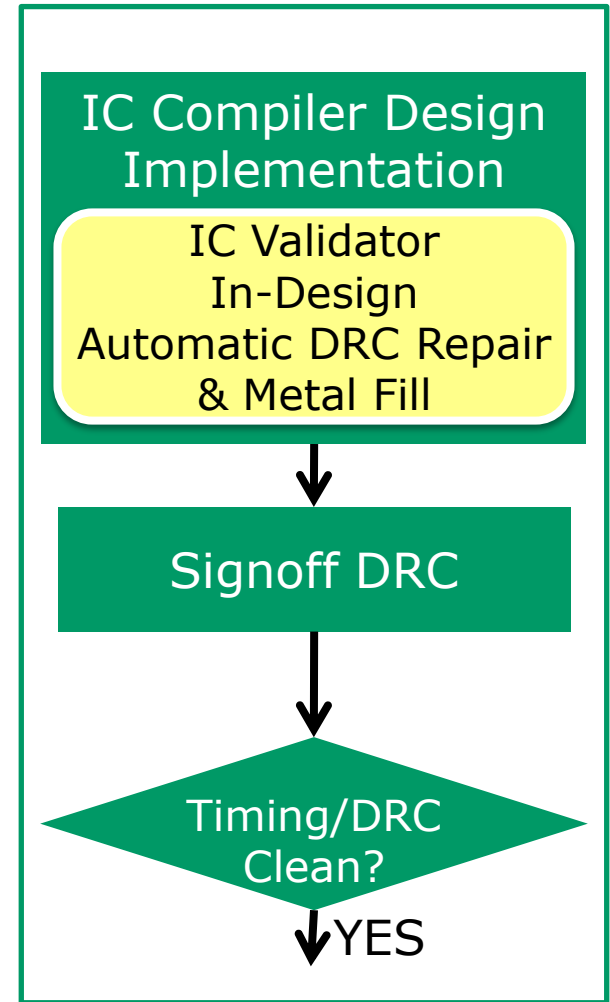
Signoff Issues at Chip Finishing

- Signoff Closure Iterations
 - Design Tool DRC correlation to Signoff DRC
 - Signoff Tool not design aware (timing / connectivity)
- Runtime
 - Hand edits are not acceptable
 - Iterating between design and signoff tools is slow



Automatic Signoff DRC Repair

- Advanced process DRC not captured in routing techfiles
 - Rules too complicated or slow for router
- Conservative routing rule has area cost
 - Allow aggressive routing
- Automated DRC Repair Requirements
 - Fast runtime
 - Electrical checks after repair (timing/IR/EM)
 - Post DRC repair ECO

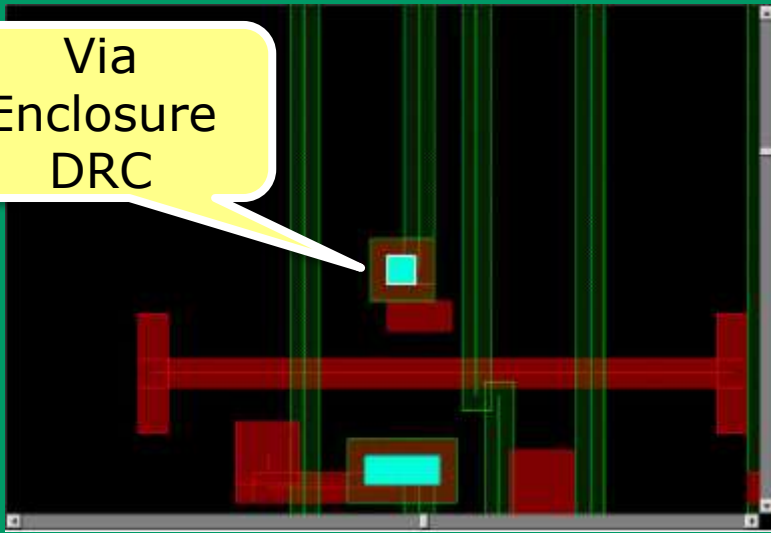


Example of Automated DRC Repair (ADR)

- DRC repaired and incrementally verified
- Timing change is minimal (within 5ps)

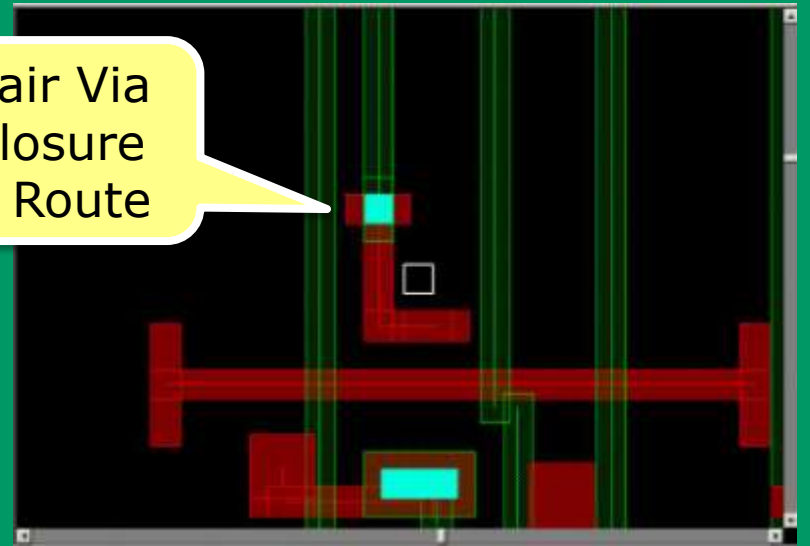
Before ADR

Via
Enclosure
DRC



After ADR

Repair Via
Enclosure
and Route



Automated DRC Repair (ADR) Evaluation

Design Details - 0.18mm², 141K nets

In-Design Results	DRC Errors	Runtime	Comments
Signoff DRC Analysis	124	10 min	1 Day of Manual Repair Effort / Timing Correlation Concern
Automatic DRC Repair	16	20 min	1 Hour of Manual Repair Effort / Improved Timing Correlation

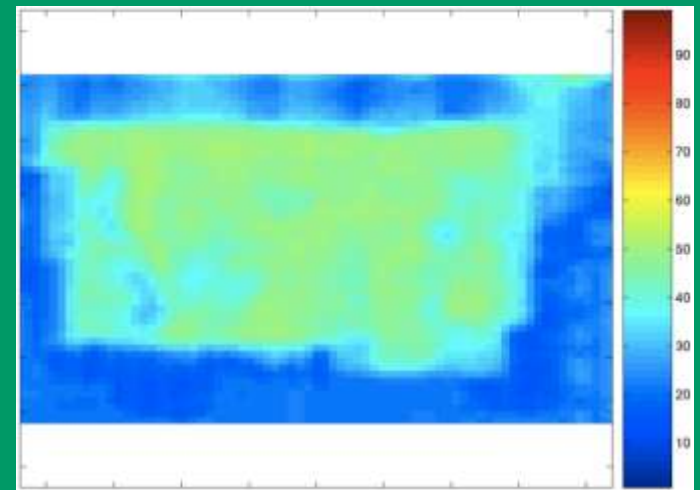
87% DRC errors fixed with ADR



Metal Fill Requirements More Complex

- Timing Aware
 - Prevent SI and timing degradation
- ECO
 - Minimize changes in metal fill during ECO routing
- Gradient Rules
 - Manage density changes between adjacent IP
 - Reduce metal variation

Reduced Metal Density Variation with Metal Fill

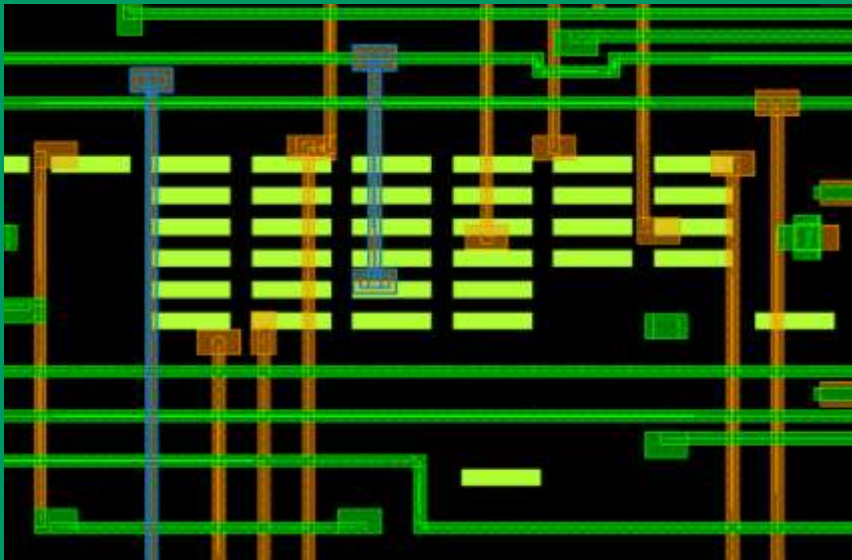


Timing Driven Metal Fill Evaluation

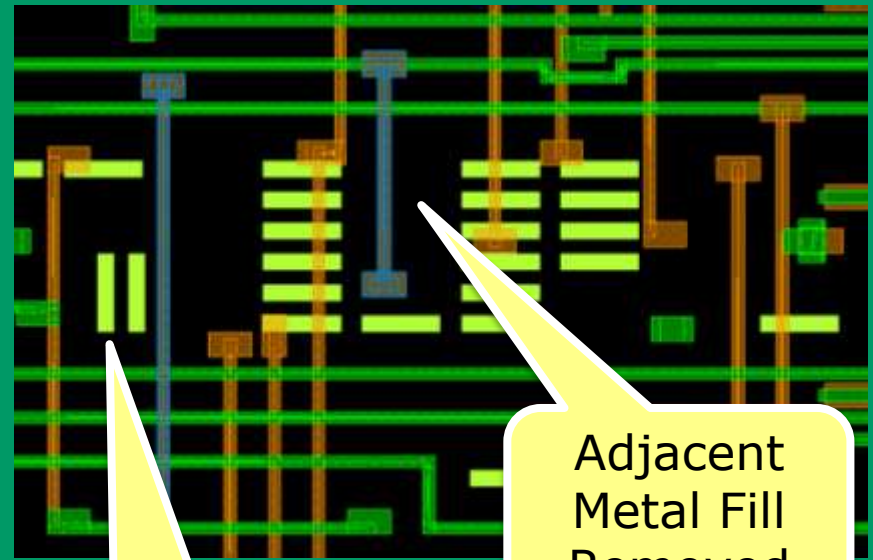
Design Details – 1.15mm², 580K nets

- Runtime 30 minutes with Foundry Supplied Techfile
- Target Density Achieved / Timing Improved

Normal Metal Fill



Timing Driven Metal Fill



Metal Fill
Added for
Density

Adjacent
Metal Fill
Removed



Next Steps and Summary

- Next Steps to Improve AMD production flow
 - More fine grained repair
 - Pattern based DRC for litho and other issues
 - CMP aware metal fill
- Benefits of physical implementation with In Design
 - Automation of DRC repair saves hours and stress
 - Tapeout Ready Design Verification (IR/EM/Timing)
 - Fastest design closure methodology

