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Predictable Success

Low Power Quick Reference Guide

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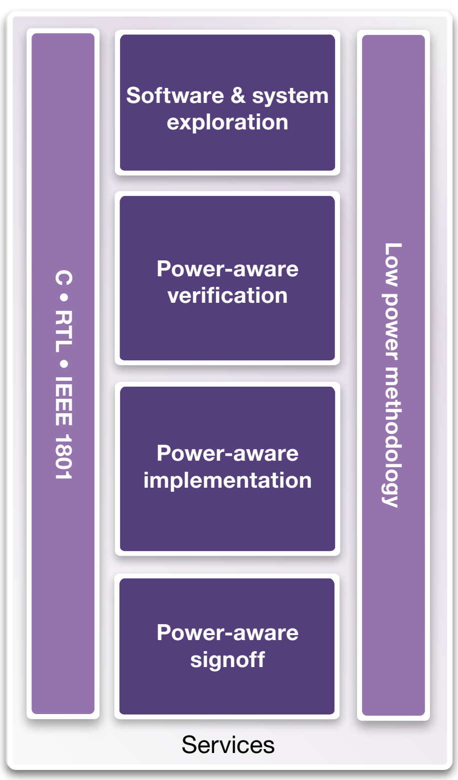
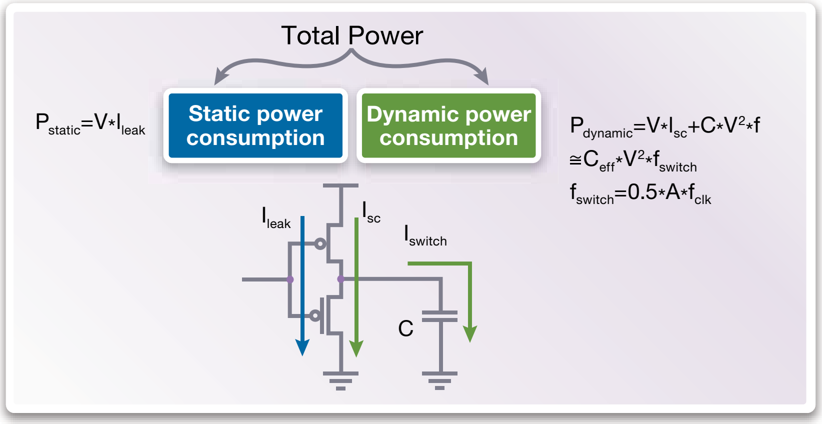
The Eclypse™ Low Power Solution delivers leading-edge, silicon-proven, advanced low power technologies in a highly automated environment. The perfect alignment of technology, methodology, IP, services, and industry standards, Eclypse Low Power Solution technology has been used in the development of the majority of today's SoCs. With over 15 years of low power technology leadership, Synopsys continues to be the ideal partner for meeting your critical power efficiency goals: longer battery life, lower cooling cost, less standby power, and ultimately, greater commercial success.



Eclypse Low Power Solution

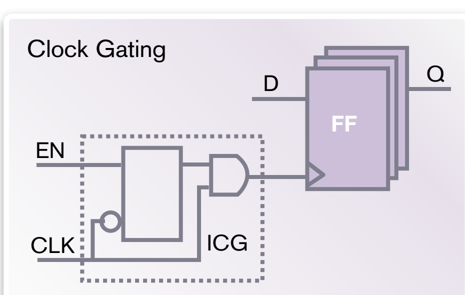
To create the most power efficient design, consideration must be given to all aspects of power consumption. Power consumption can be divided into two aspects:

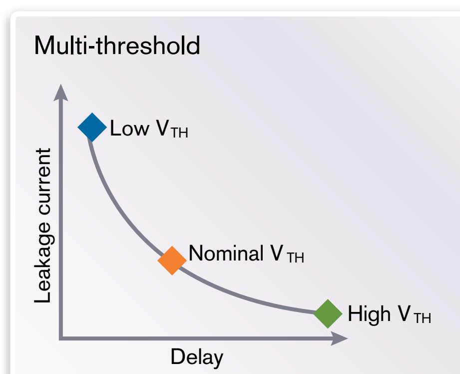


Dynamic power—the power that is consumed by a device when it is actively switching from one state to another. Dynamic power consists of switching power, consumed while charging and discharging the loads on a device, and internal power (also referred to as short circuit power), consumed internal to the device while it is changing state.

Leakage power—the power consumed by a device not related to state changes (also referred to as static power). Leakage power is actually consumed when a device is both static and switching, but generally the main concern with leakage power is when the device is in its inactive state, as all the power consumed in this state is considered "wasted" power.

Various techniques have been developed to reduce both dynamic and leakage power. The two most common traditional, mainstream techniques are:



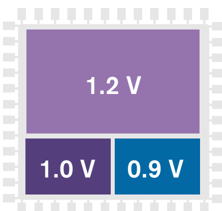


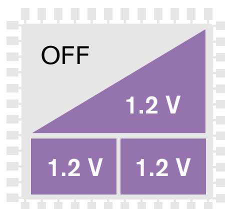
Clock gating—the disconnecting of the clock from a device it drives when the data going into the device is not changing. This technique is used to minimize dynamic power.

Multi-Vth optimization—the replacement of faster Low-Vth cells, which consume more leakage power, with slower High-Vth cells, which consume less leakage power. Since the High-Vth cells are slower, this swapping only occurs on timing paths that have positive slack and thus can be allowed to slow down.

As technologies have shrunk, leakage power consumption has grown exponentially, thus requiring more aggressive power reduction techniques to be used. Similarly, clock frequency increases have caused dynamic power consumption of the devices to outstrip the capacity of the power networks that supply them, and this becomes especially acute when high power consumption occurs in very small geometries, as this is a power density issue as well as a power consumption issue.

Several advanced low power techniques have been developed to address these needs. The most commonly adopted techniques today are:





Multi-voltage (MV)—the operation of different areas of a design at different voltage levels. Only specific areas that require a higher voltage to meet performance targets are connected to the higher voltage supplies. Other portions of the design operate at a lower voltage, allowing for significant power savings. Multi-voltage is generally a technique used to reduce dynamic power, but the lower voltage values also cause leakage power to be reduced.

Power gating—the complete shut off of supply nets to different areas of a design when they are not needed (also known as MTCMOS or power shutdown). Since the power has been completely removed from these shutdown areas, the power for these areas is reduced essentially to zero. This technique is used to reduce leakage power.

It is very common to see multi-voltage and power gating used together on the same design, whereby different regions operate at different voltages, and one or more of those regions can also be shutdown.

For more information on advanced low power techniques, see the glossary.

Adaptive Voltage Scaling (AVS)
A closed loop extension to Dynamic Voltage-Frequency Scaling. A power control functional block/monitor within the design scales voltage dynamically according to varying workloads. Process variation and temperature are taken into account as the monitor is on-silicon.

Back Biasing
(See Well Biasing)

Clock Gating
Clock gating is a mainstream low power design technique targeted at reducing dynamic power by disabling the clocks to inactive flip-flops.

Dynamic Voltage and Frequency Scaling (DVFS)
Modifying the operating voltage and/or frequency at which a device operates, while it is operational, such that the minimum voltage and/or frequency needed for proper operation of a particular mode is used.

Isolation
Isolation is a technique for controlling the behavior of a signal that is driven into or out of a powered down power domain. Isolation consists of driving the signal to a known state—1, 0, or latching it to a previous value—when the power domain is powered down.

Multi-Corner, Multi-Mode (MCMM) (also known as Multi-Scenario)
Multi-corner, multi-mode considers optimization and analysis at multiple operating corners, and in multiple operational modes, concurrently, instead of using an iterative process that may never converge.

Multi-Threshold CMOS (MTCMOS)
MTCMOS refers to a circuit scheme in which two types of transistors are used: low threshold voltage transistors capable of higher performance due to faster switching speeds, and high threshold voltage transistors that consume less leakage power. Coarse- and fine-grain MTCMOS refer to global and local sleep transistor allocation, respectively. The term “MTCMOS” is also commonly used interchangeably with the term “power gating”. (See also Power Gating)

Multi-Voltage
Multiple voltage rails (multi-Vdd) can be supplied to a design to impact power and performance. A higher voltage yields a faster circuit, but with higher dynamic power. In many designs, only discrete portions of the design need to run at high speed. Other portions may operate at lower speeds, and thus require lower voltages (and therefore consume less power).

Multi-Voltage Threshold (Multi-Vth)
An optimization performed to minimize leakage power by substituting cells that have higher voltage thresholds in place of cells that have lower voltage thresholds. Higher voltage threshold cells dissipate less leakage power, but operate slower than lower voltage threshold cells. Hence, multi-Vth optimization is a tradeoff between leakage power and path timing.

Power Domain
Power domains are areas in the design that are grouped by common power environments and power strategy, such as for power down conditions, operating voltage, power supply nets, etc.

Power Gating
Power gating uses high-Vth “sleep transistors” (also referred to as power switches) to disconnect power supplies to higher-speed and higher-power logic when that logic is not being actively used. Power can be gated using either header cells (which disconnect the Vdd) or footer cells (which disconnect the Ground).

State Retention
Capability to retain the critical state sequential elements within a block when the block is powered down. State retention generally requires saving the registers and possibly memory contents of the block.

Unified Power Format (UPF) (IEEE-1801)
The IEEE-1801 (Unified Power Format) is an open industry standard for the specification of implementation-relevant power information early in the design process RTL (register transfer level) or earlier.

Voltage area
A physical representation of a power domain. Generally, it is recommended to have a one-to-one correspondence between power domains and voltage areas, although this is not a requirement.

Variable Threshold CMOS (VTCMOS)
Variation of the well voltage to adjust threshold voltage, which in turn increases speed (forward bias) or reduces leakage (backward bias). Also known as Variable Vth. (see well biasing).

Well Biasing
Separate voltage supplies can be used to connect to the NMOS and PMOS bulk regions in triple well CMOS technologies. Modification of these voltages with respect to the primary power and ground supplies is called well-biasing. These supplies can be modulated to provide a back-bias voltage which causes an increase in device Vth, reducing the sub-threshold leakage. These supplies can also be modulated in the reverse direction to provide a forward-bias voltage which causes a decrease in device Vth that increases the speed at which the transistors switch, at a cost of increased sub-threshold leakage. Thus, well-biasing can be used to directly adjust between high performance and low power consumption.

Resources

For more information, visit http://www.synopsys.com/eclypse or download any of the following items:

White papers

- Synopsys Eclypse Low Power Solution
  http://tinyurl.com/2f7lu2d
- Hybrid Techniques Reduce Dynamic Power Consumption
  http://tinyurl.com/2basxhm
- Pain Management in Power Optimization
  http://tinyurl.com/2daggbm

Video

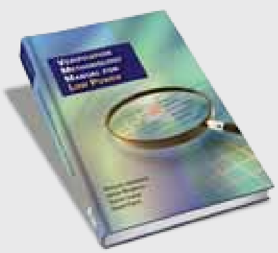
- Godwin Maben: Low Power Trends and Methodology
  http://tinyurl.com/2eqzt5s

Webinars

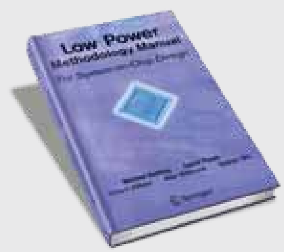
- Static Verification Throughout the Low Power Design Flow
  http://tinyurl.com/282a79k
- Low Power Architecture Exploration for ASIC Algorithm Implementation
  http://tinyurl.com/23dv5qa

Article

- Low Power Design is Here to Stay
  http://tinyurl.com/26gdc8y



VMM-LP: In response to the increasing need for targeted verification of low-power IC designs, the Verification Methodology Manual for Low Power Design (VMM-LP) is now available. VMM-LP is a companion book to the Verification Methodology Manual (VMM) for SystemVerilog, which provides proven industry best practices developed since 2005. The VMM-LP methodology addresses all aspects of functional verification for designs employing power management strategies and techniques. Synopsys' corresponding implementation of the VMM-LP base class library is also freely available. Current Synopsys customers can also download a free PDF copy of the VMM-LP at www.vmmcentral.org/lowpower.html.



LPMM: The "Low Power Methodology Manual" (LPMM) is a comprehensive and practical guide to managing power in system-on-chip designs, critical to designers using 90-nanometer and below technology. Combining extensive commercial experience, deep scientific understanding, silicon technology case studies, and a pragmatic approach, the manual describes design techniques which address both dynamic and static (leakage) power, including methods for power gating and dynamic voltage and frequency scaling. Current Synopsys Customers can download a free PDF copy of the LPMM at www.lpmm-book.org.