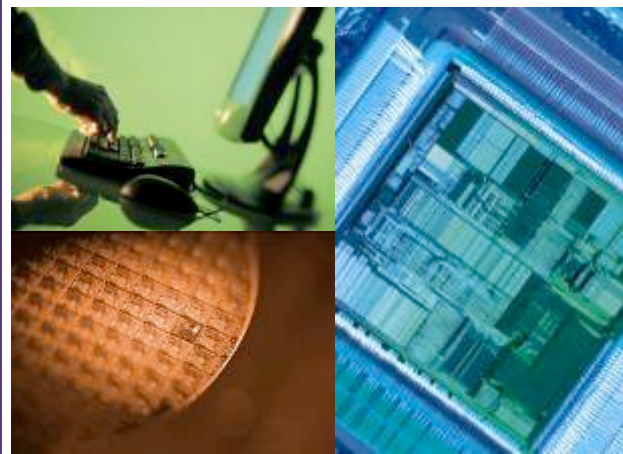


# Design and Verification of Ultra Low Power SoCs with ARM Cores

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Group Director, R&D, VG

Prapanna Tiwari  
CAE Manager, VG



# Agenda

- Introduction
- Common Power Management schemes on ARM based SOCs
- Typical errors found in power management
- Bug Avoidance and Verification Strategy
- Conclusion

# Introduction

# Making the leading solution in Power Management Verification

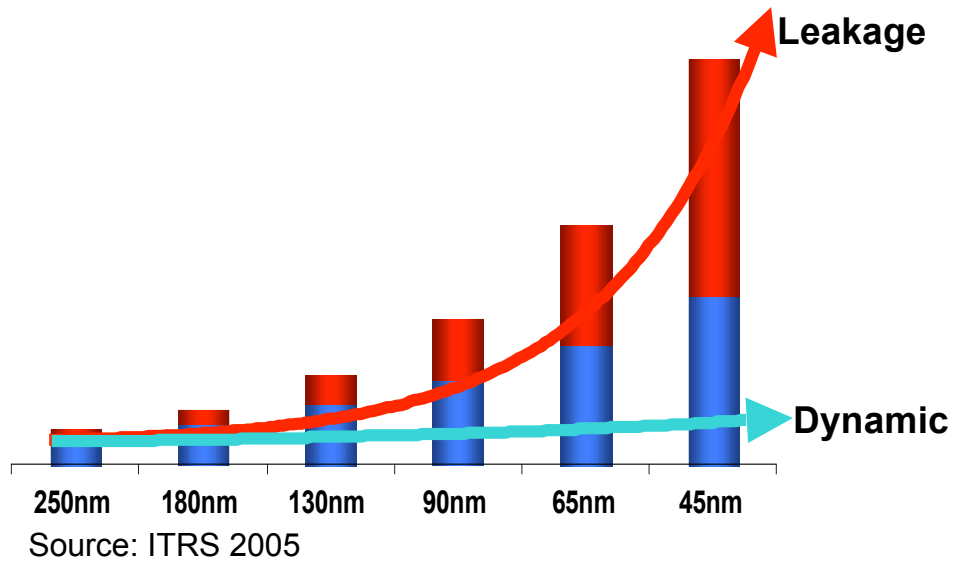
## SYNOPSYS ACQUIRES ARCHPRO DESIGN AUTOMATION

*ArchPro's Power Management Technologies to Enhance Synopsys' Low Power Design and Verification Solution*

**MOUNTAIN VIEW, Calif., June 18, 2007** - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, today announced that it has acquired ArchPro Design Automation. ArchPro's technologies enable engineers to address power management challenges in multi-voltage designs from architecture to RTL to gates..

**"ArchPro's industry-leading technologies are actively used in verification and sign-off of our most advanced multi-voltage designs,"** said Hisaharu Miwa, general manager, Design Technology Div, LSI Product Technology Unit at Renesas Technology Corp. "Use of innovative low-power design techniques continues to increase rapidly at Renesas. Integration of Synopsys' market-leading verification technologies including SystemVerilog testbenches, coverage, and assertions with ArchPro's advanced power management verification techniques will create a unique value-proposition for addressing the exponentially growing verification challenge."

# Power is a huge challenge for IC design



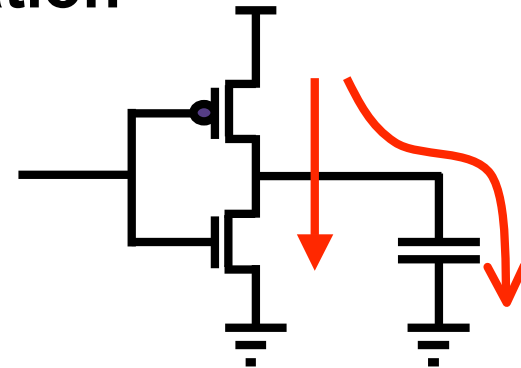
**Both dynamic and leakage power are problematic**

# Dynamic Power Dissipation

$$P_{dynamic} = P_{switching} + P_{shortcircuit}$$
$$= (0.5 \times C \times V^2 \times \alpha \times f) + (I_{sc} \times V)$$

## To reduce dynamic power dissipation

- Reduce voltage
- Reduce capacitance
- Reduce switching activity



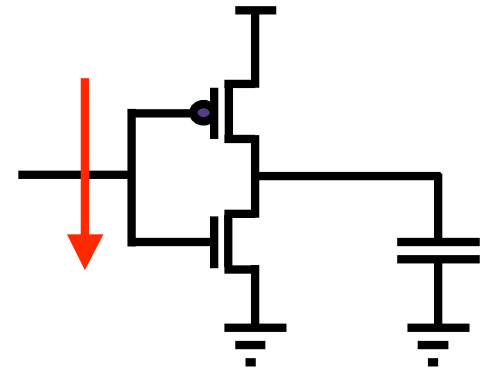
**Voltage control is key**

# Static Power Dissipation

$$P_{leakage} = (I_{sub-threshold-leakage} \times V) + (I_{gate-oxide-leakage} \times V)$$
$$= (K_1 W e^{-V_{th}/nV_e} (1 - e^{-V/V_e}) \times V) + (K_2 W (V / T_{ox})^2 e^{-\alpha T_{ox}/V} \times V)$$

## To reduce static power dissipation

- Reduce voltage
- Increase threshold voltage
- Improve process technology



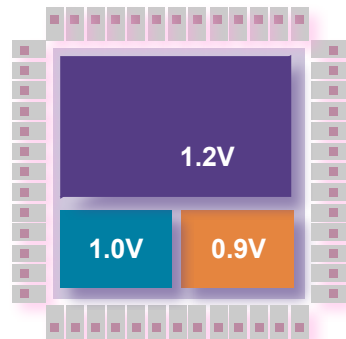
**Voltage control is key**

# Power Management Techniques

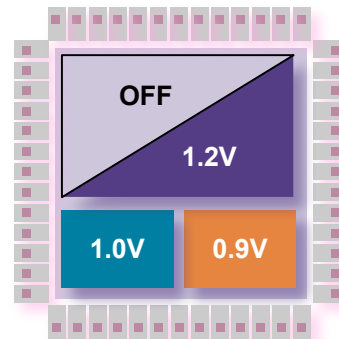
- Dynamic Power
  - Reduce Voltage
  - Reduce Capacitance (Small Transistors, Short Wires)
  - Reduce Switching activity (Clock-Gating, Sleep Mode)
- Static Power
  - Reduce Voltage
  - Increase threshold voltage (Use of High  $V_t$  transistors)
  - Specialize manufacturing process technology

**Voltage control techniques can result in up to 2X/10X savings in power**

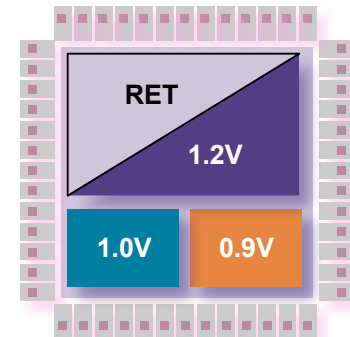
# Voltage-Control Techniques



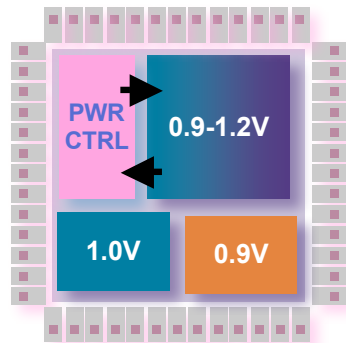
Multi-Voltage (MV)



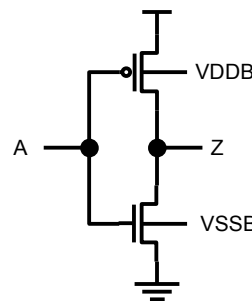
MTCMOS power gating (shut down)



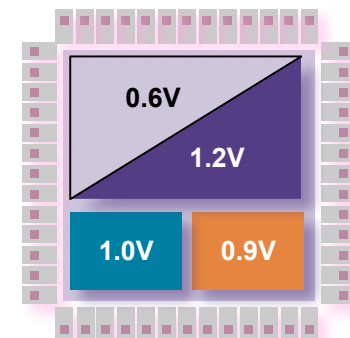
Power gating with State Retention



Dynamic or Adaptive Voltage Frequency Scaling (DVS, DVFS, AVS, AVFS)

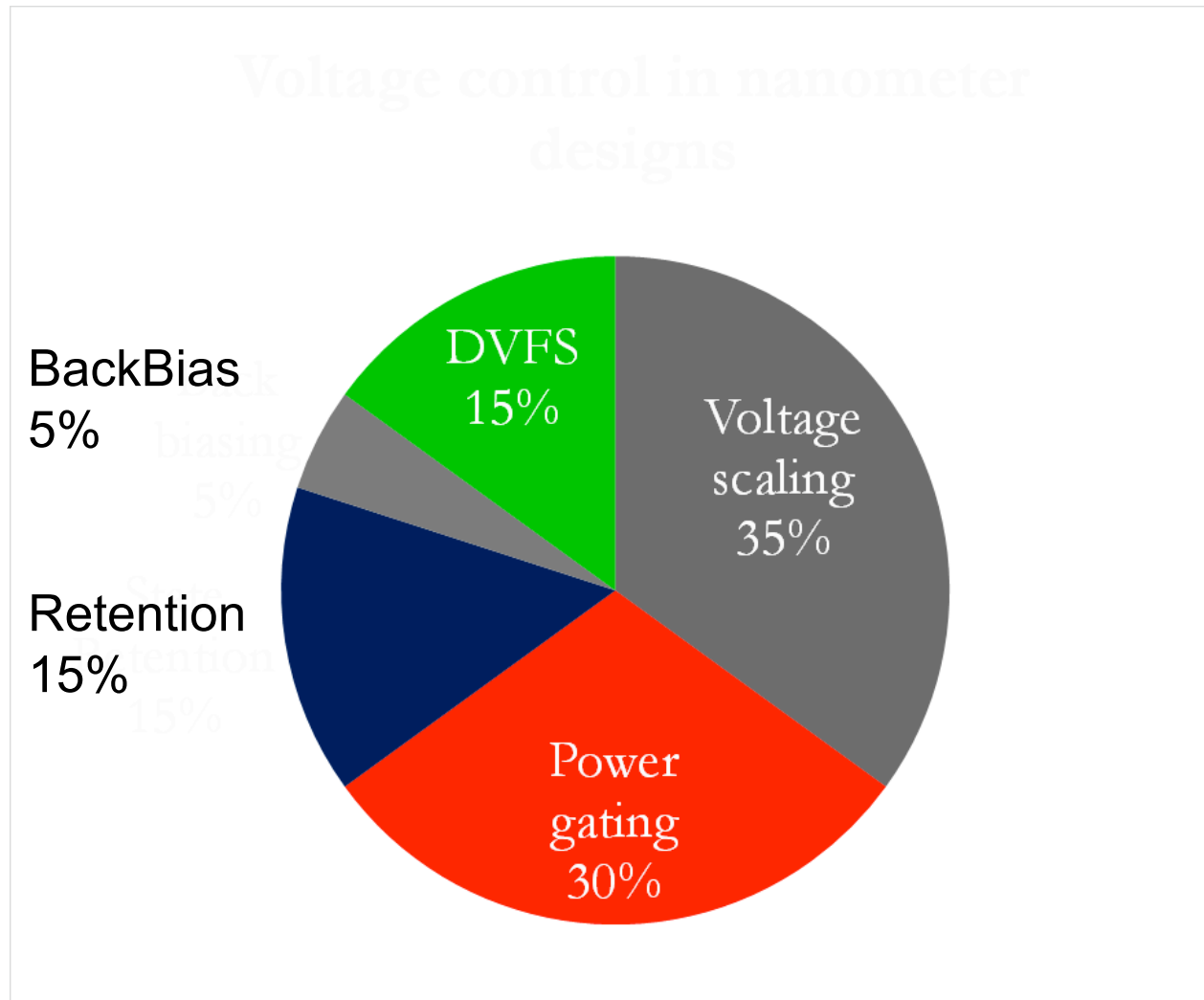


Variable  $V_{TH}$  (Back Bias – P/N)



Low-VDD Standby

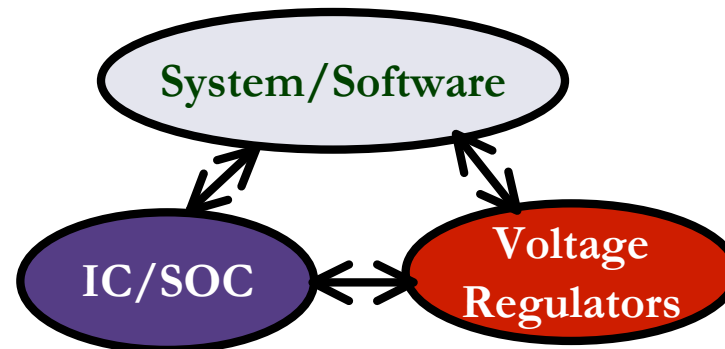
# Voltage Control Has Become The #1 Choice for Power Reduction



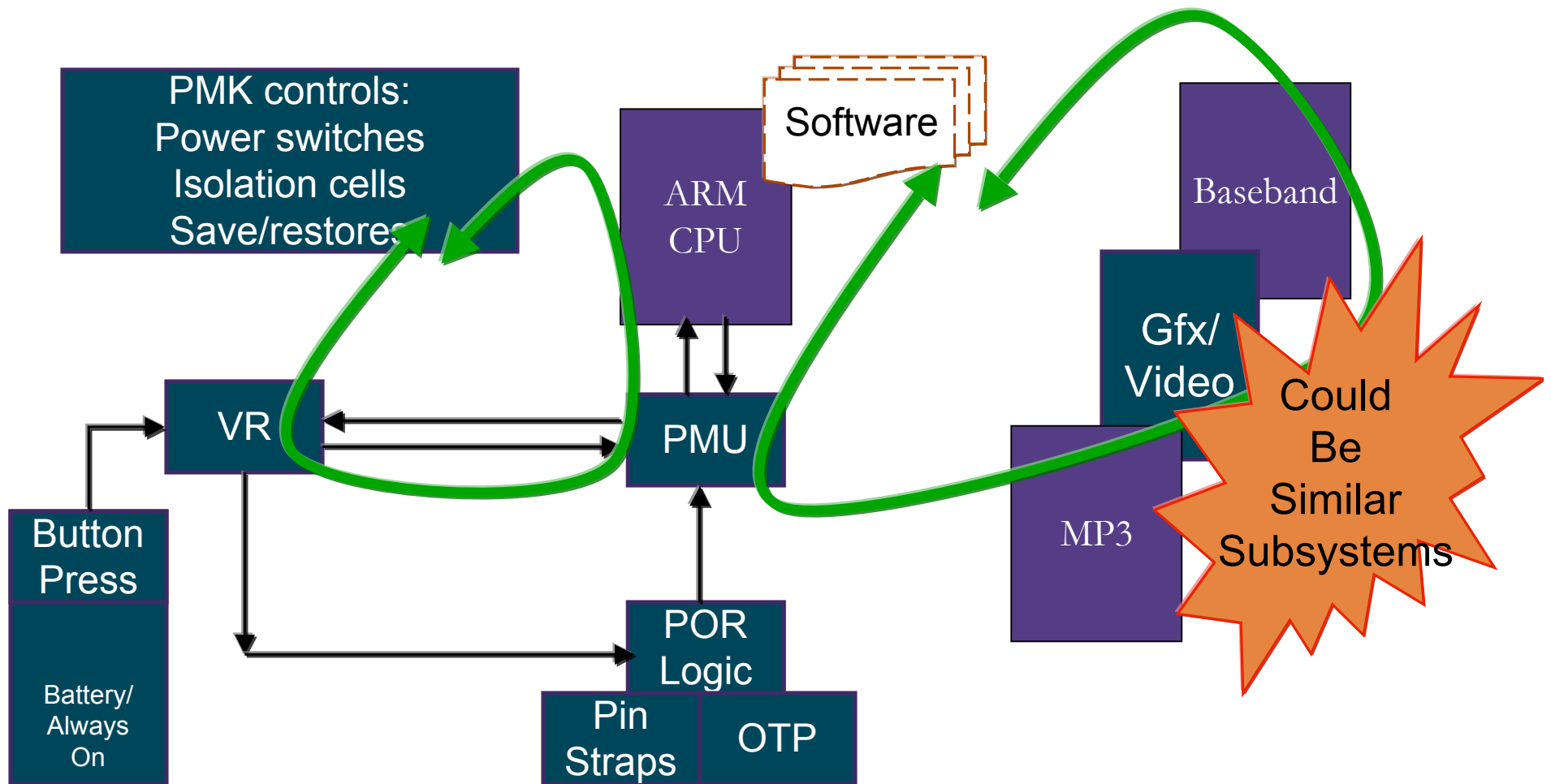
# Common Power Management Architectures

# A typical mobile SOC ...

- Consists of
  - One or more ARM cores
  - Blocks(Islands) that can be independently controlled
    - Plus, Voltage Regulators/Power Switches etc.
  - A hardware power management unit
  - A software driver for power management functions
  - Both Hardware and Software Inputs to the PMU



# A typical mobile SOC



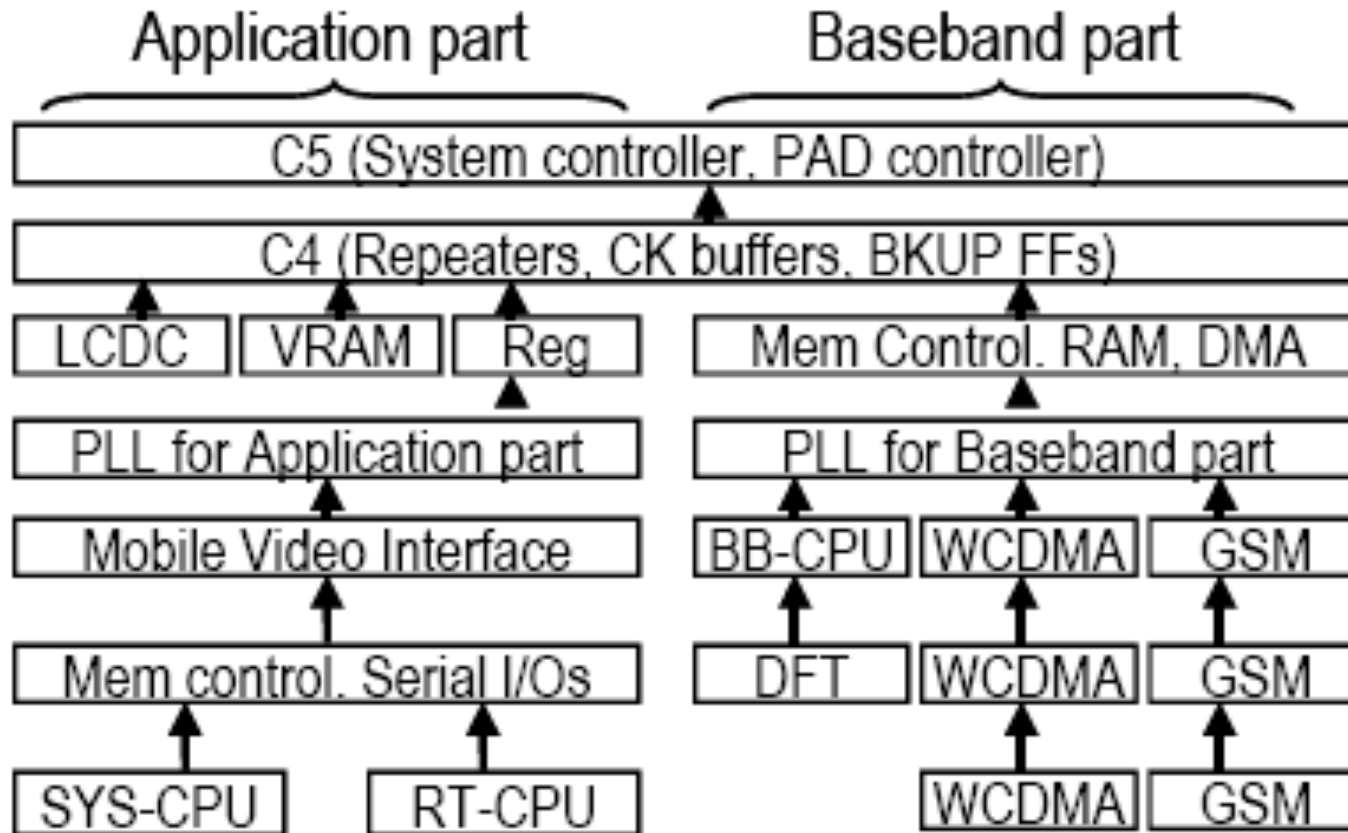
# e.g. Smart Phone Wakeup

- Button Press – H/W initiated
  - Activates various parts – keyboard, screen, password routine etc.
- Alarm Clock – S/W initiated
  - Software initiated wakeup on some programmable interrupt function

**In reality, h/w and s/w interplay with each other**

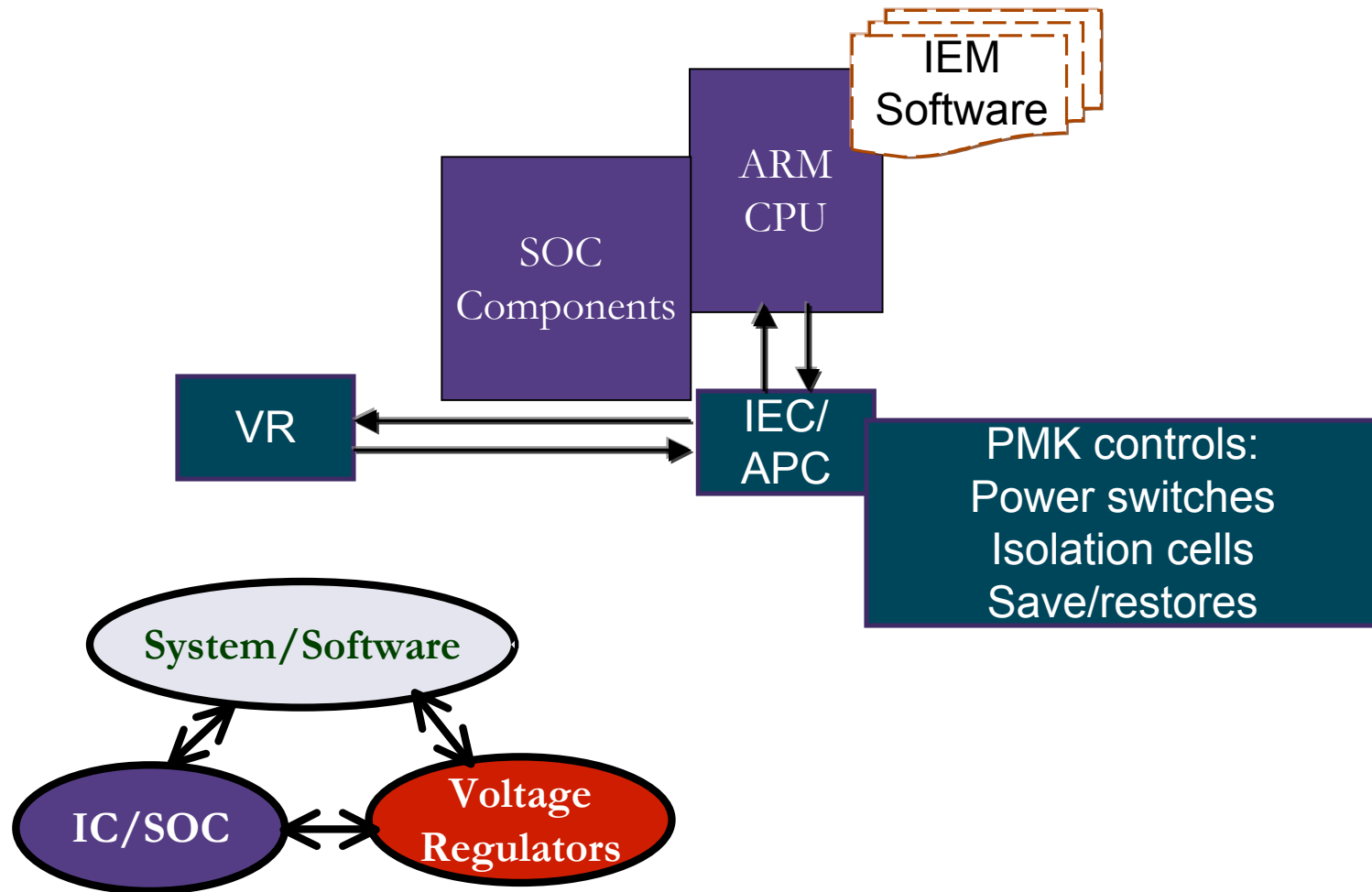
**There could be multiple events in parallel**

# An Example SmartPhone



Reference - Hierarchical Power Distribution and Power Management Scheme for a Single Chip Mobile Processor -Toshihiro Hattori, et.al, DAC2006, pg 292

# ARM IEM – A ready to use h/w-s/w solution- silicon proven



# ARM-Synopsys\* Collaborate to Verify IEM+926 based SOC, 06/2005

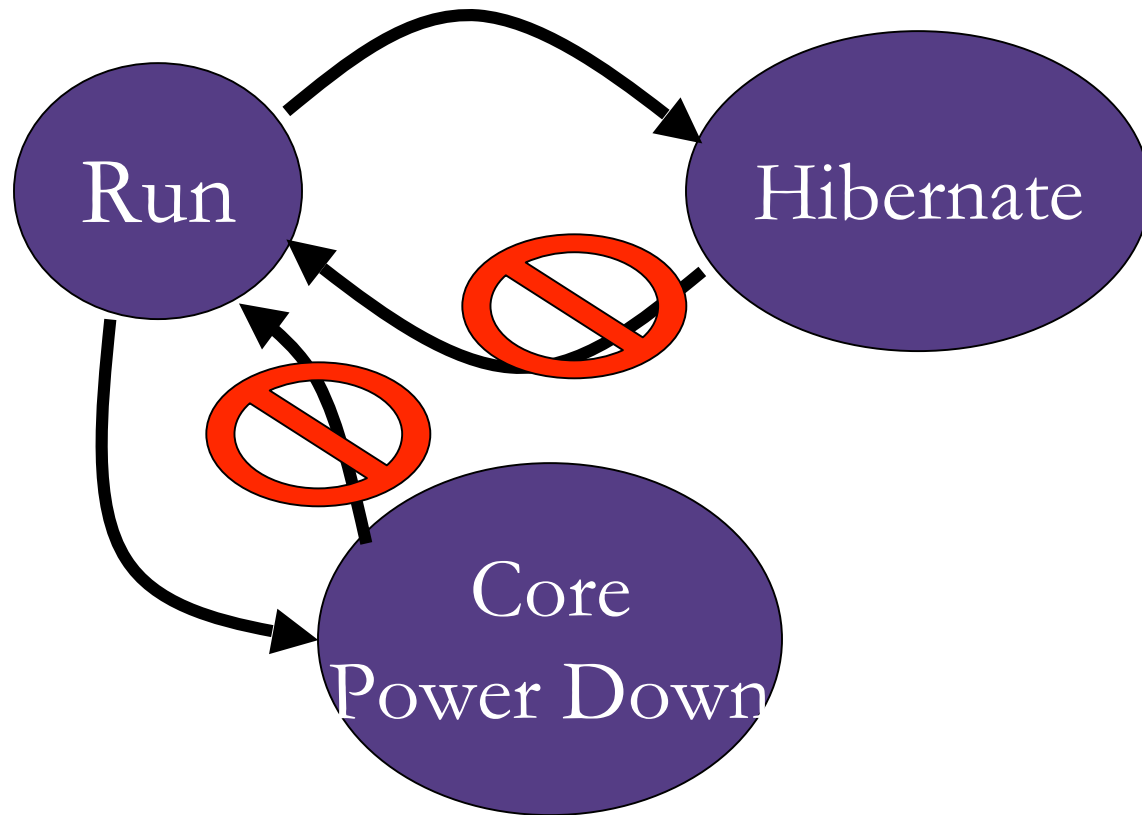
- 65nm CPU, 3 voltage domains, ARM926 based SOC
  - AVFS, Back Bias, Standby, Power Gating, Retention techniques applied
  - IEM Hardware/Software controller
- 60% dynamic power savings, 8x-10x leakage reduction demonstrated

Completely verified at the RTL and Netlist stages: resulting in first pass silicon success

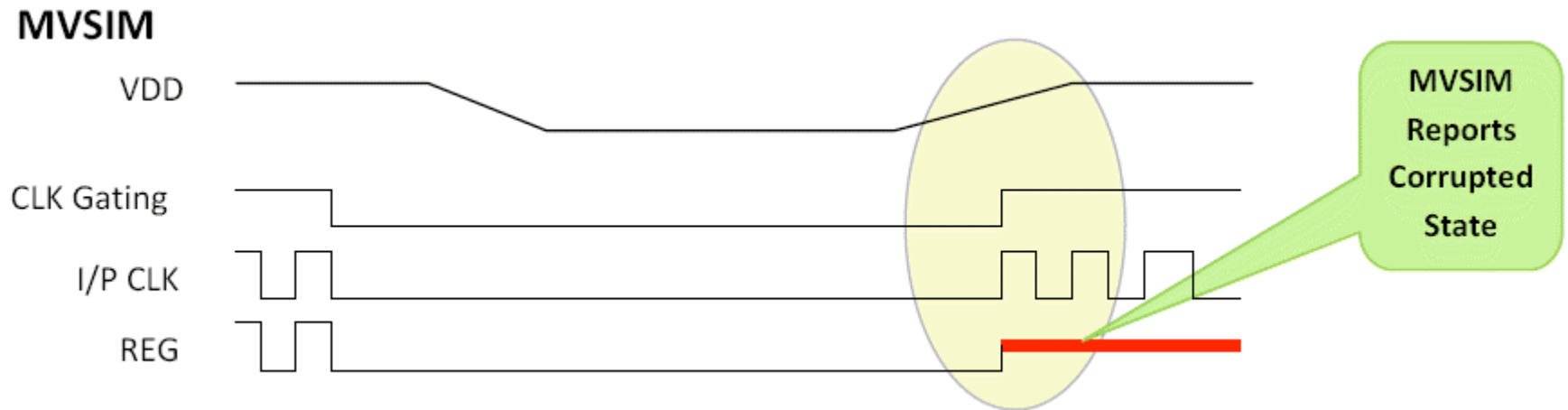
\* ArchPro products were used at that time

# Typical Error Situations

# Failure to Wakeup



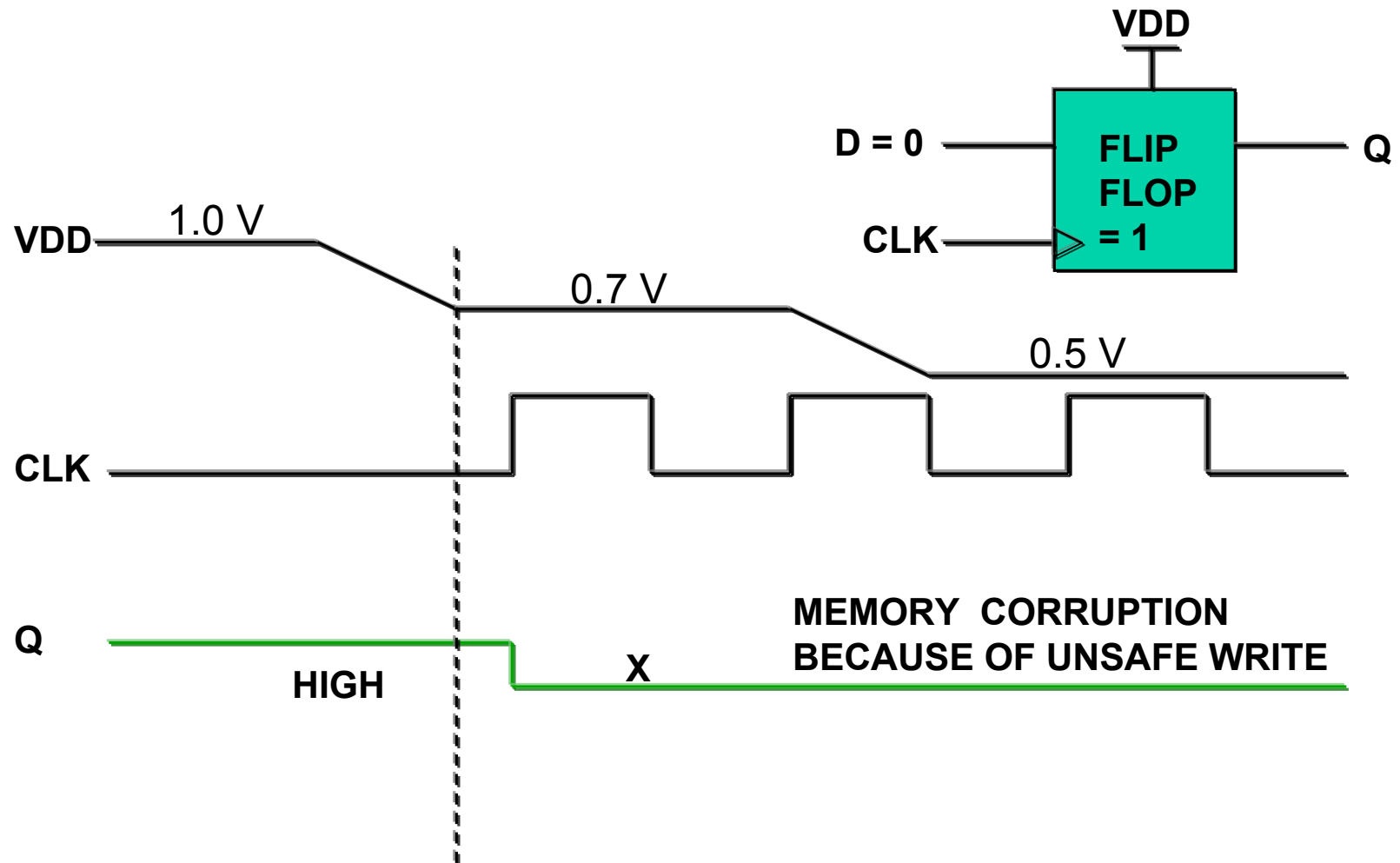
# Premature Write → Can't wake up from Hibernate



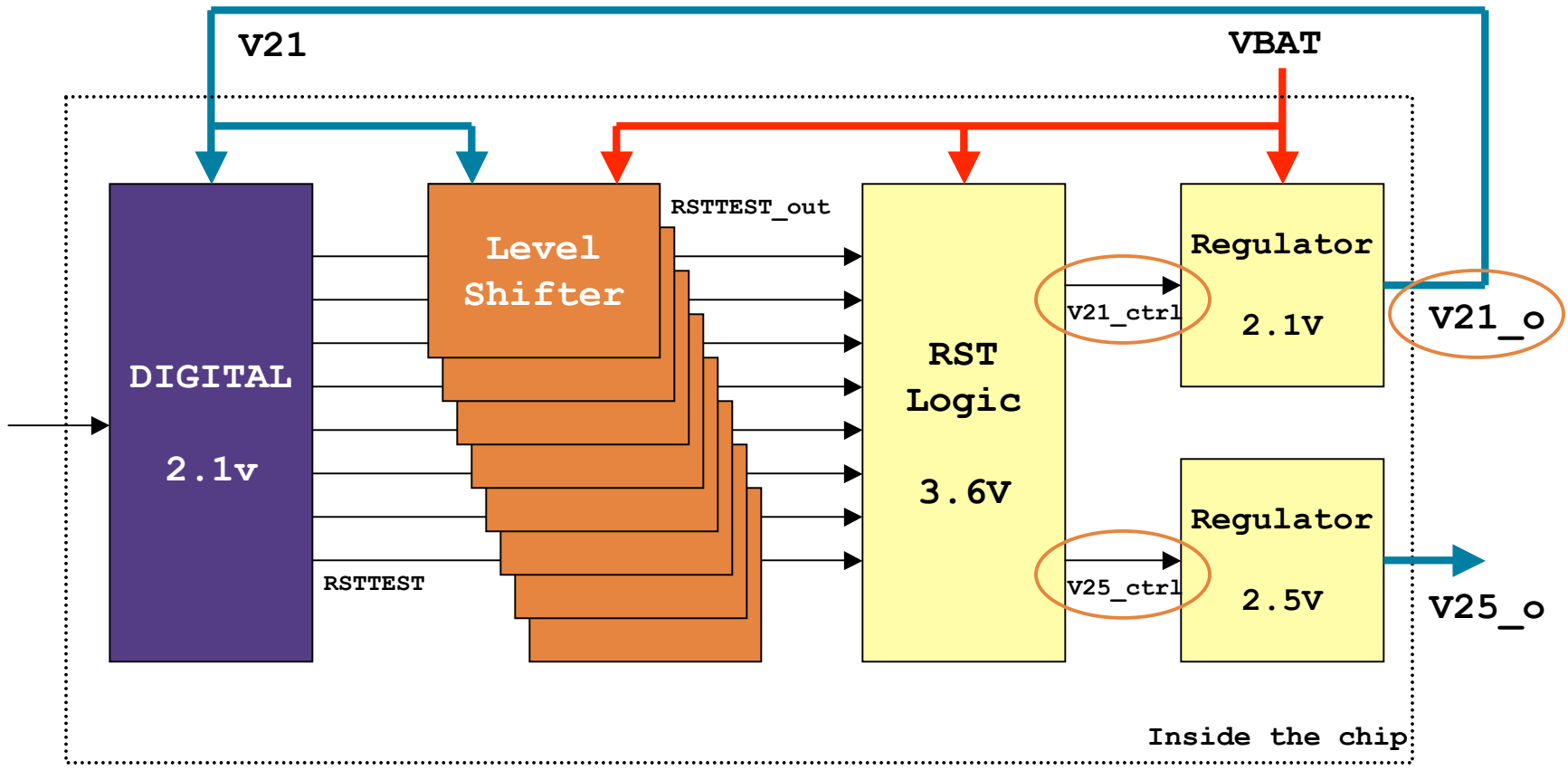
CLK Gating Signal released prematurely  
Insufficient voltage for write  
Unknown value in REG leading to memory corruption

Traditional simulators will not detect this issue because they can't simulate a voltage ramp

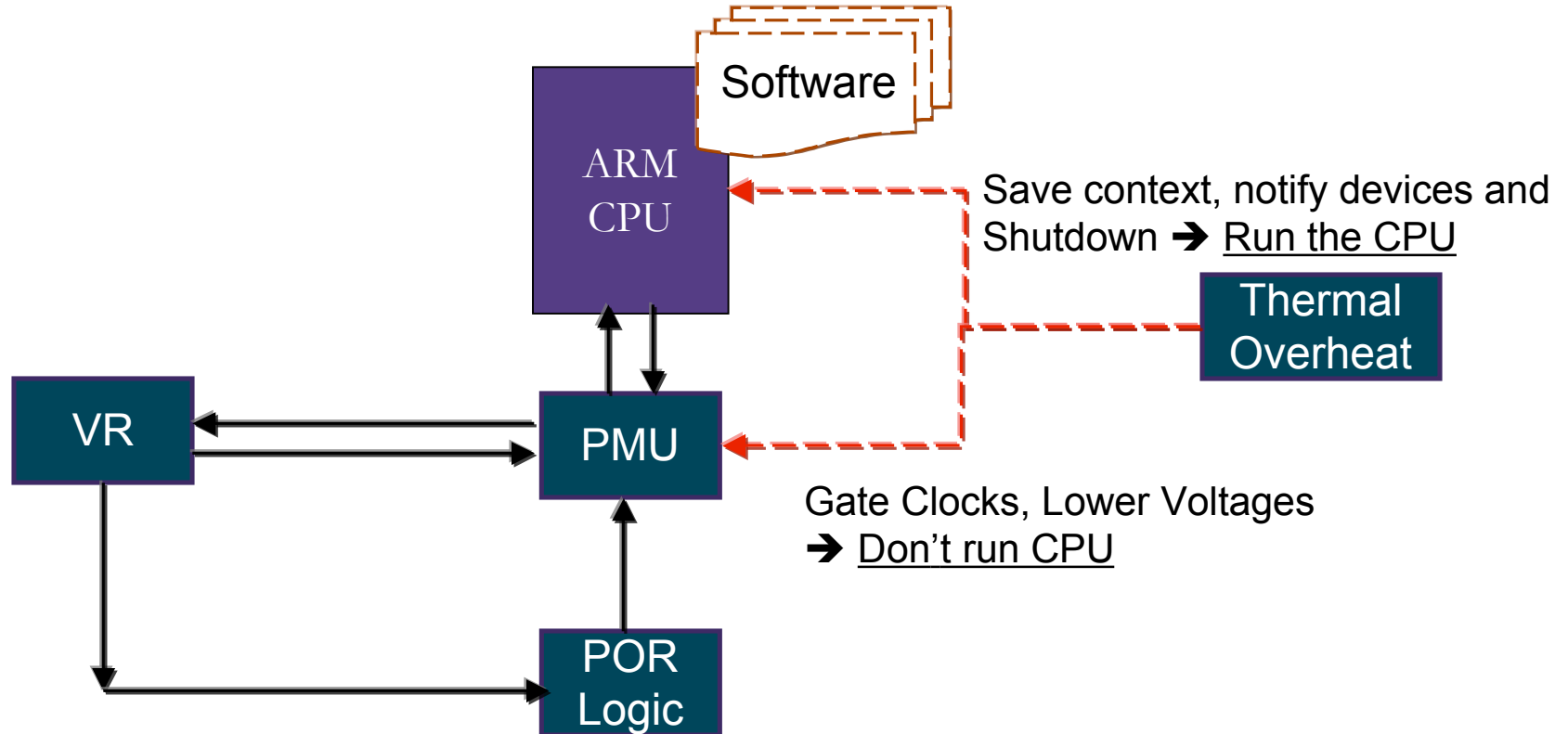
# Unsafe Writes → Memory Corruption



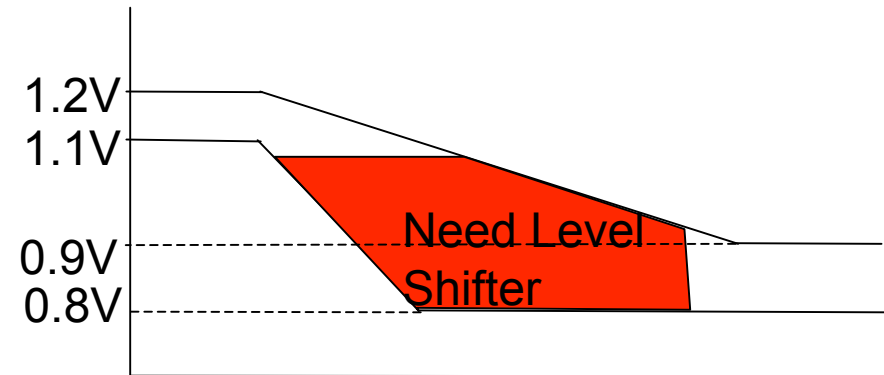
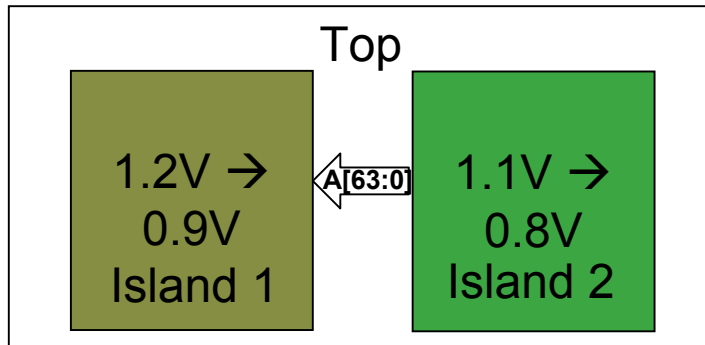
# Using Off islands to Wakeup!



# Conflicting events!



# Voltage Scheduling Error

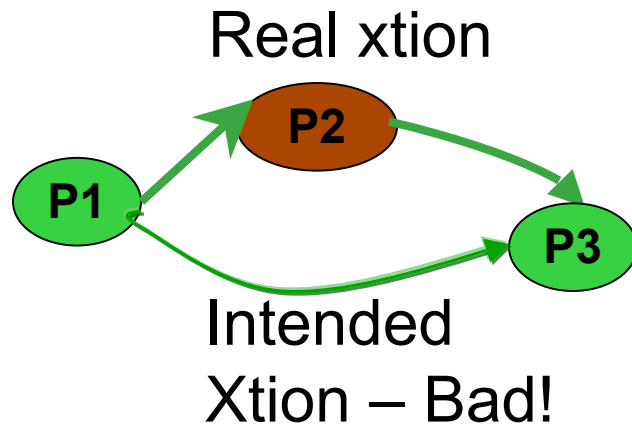


Power State Table		
V1	V2	Need LS?
1.2V	1.1V	No
0.9V	0.8V	No

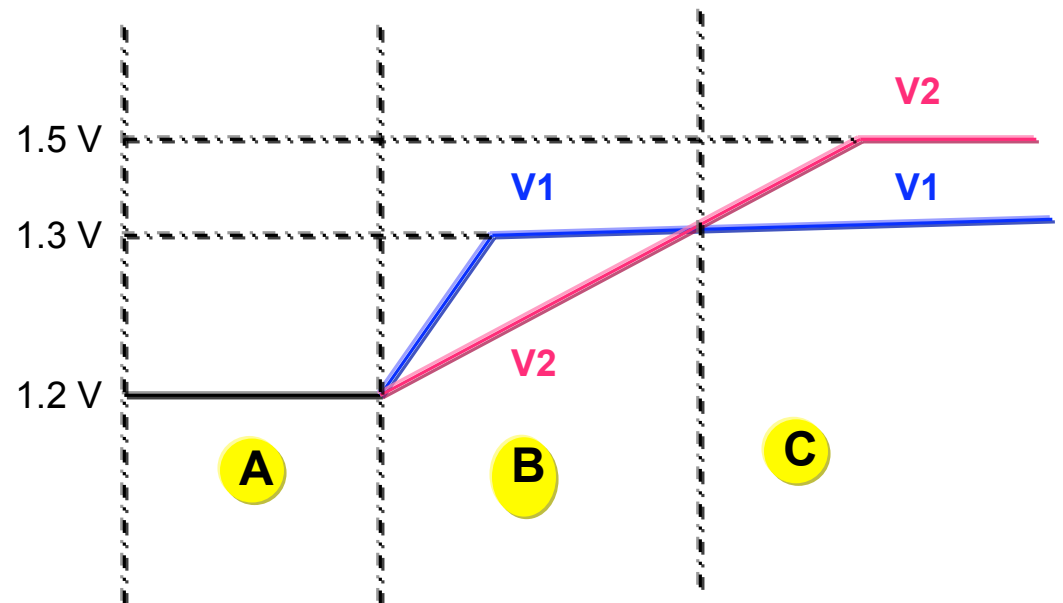
Dynamic Situation – Need level shifter or change Voltage Scheduling

Static Analysis – No level shifter needed

# Bad xtions and Intermediate states

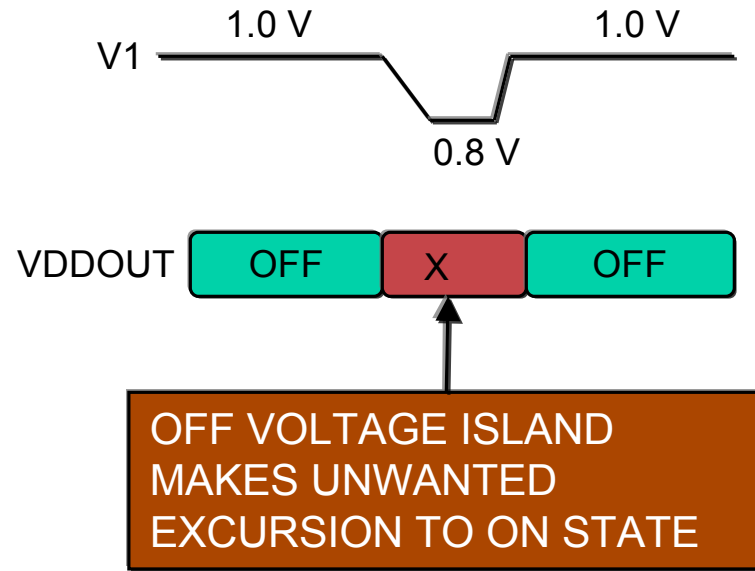
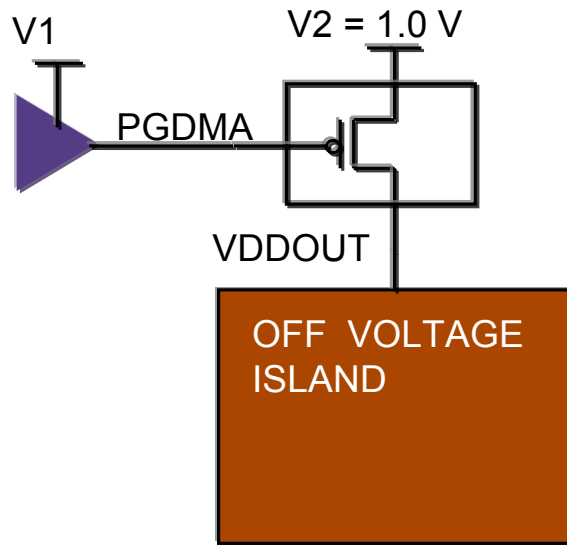


Power State Table		
Power State	V1	V2
P1	1.2V	1.2V
P2	1.??V	1.?? V
P3	1.3V	1.5V

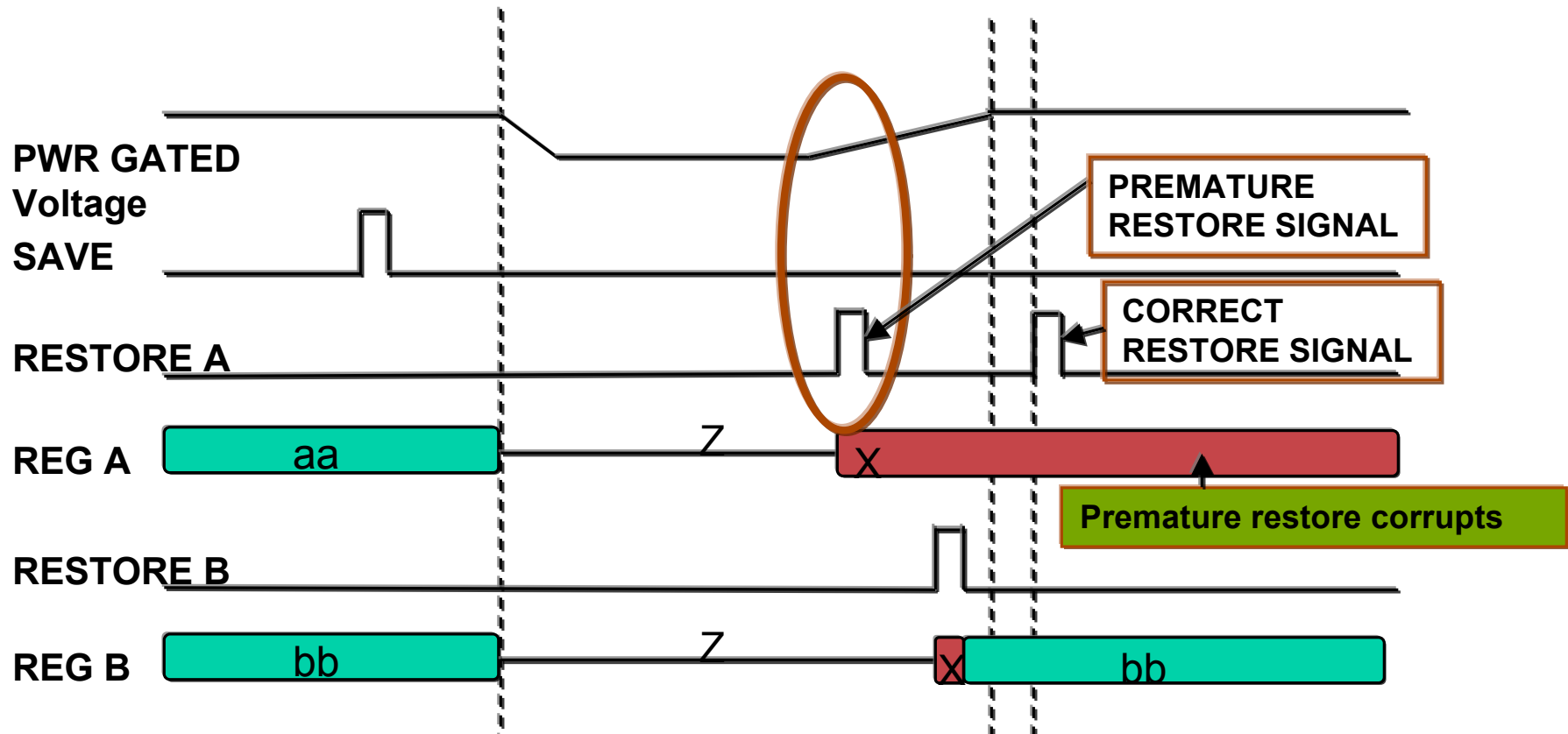


	V1 -> V2	V2 -> V1
<b>A</b>	No Level Shifter Needed	
<b>B</b>	H2L	L2H
<b>C</b>	L2H	H2L

# Unplanned State causes Power Gating Collapse



# Premature Restore : Don't race against Voltage



**Sensing Voltage Readiness is really tricky!**

# Combining Multiple CPUs

- Must take a hierarchical sub-system view
- Must be conscious of s/w threads and h/w events in each sub-system
- An “FSM” view of power states must be commonly known across the sub-system boundary
  - E.g ACPI
- Best to enforce a consistent protocol across all sub-systems
  - Industry standards are only emerging here
- Homogeneous subsystems make code-reuse possible
  - A draw back of heterogeneous subsystems, but this is common

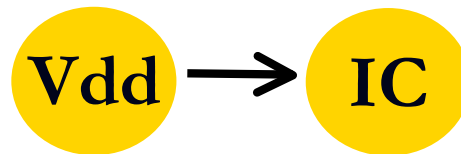
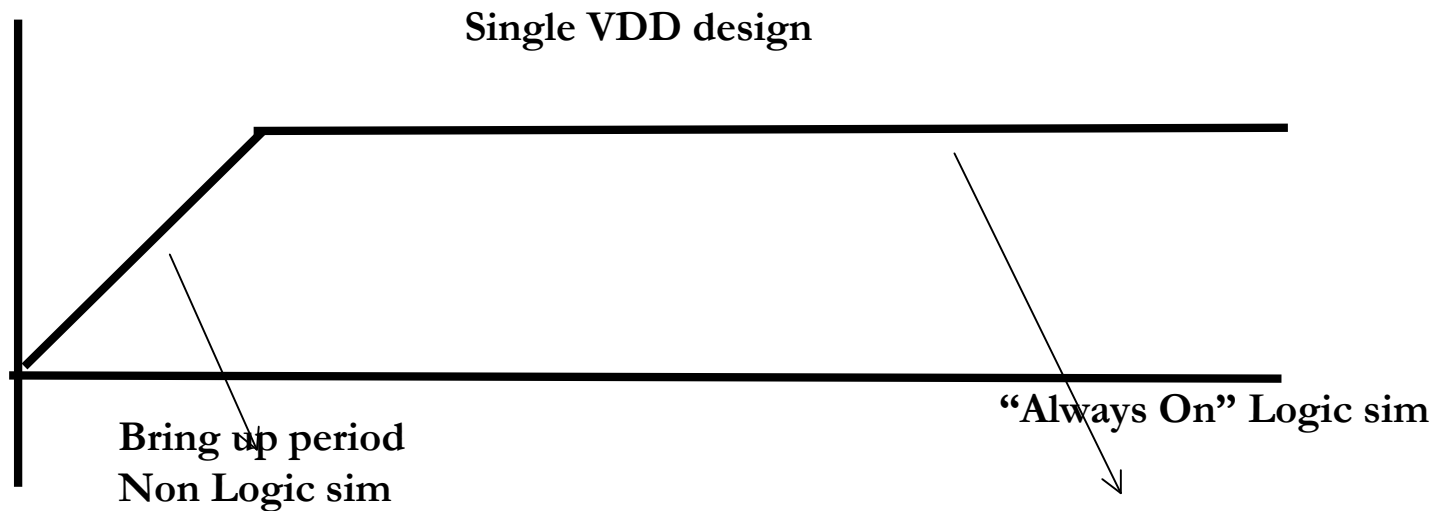
# Bug Avoidance and Verification Strategy

# 2 dimensions of Power Management Verification

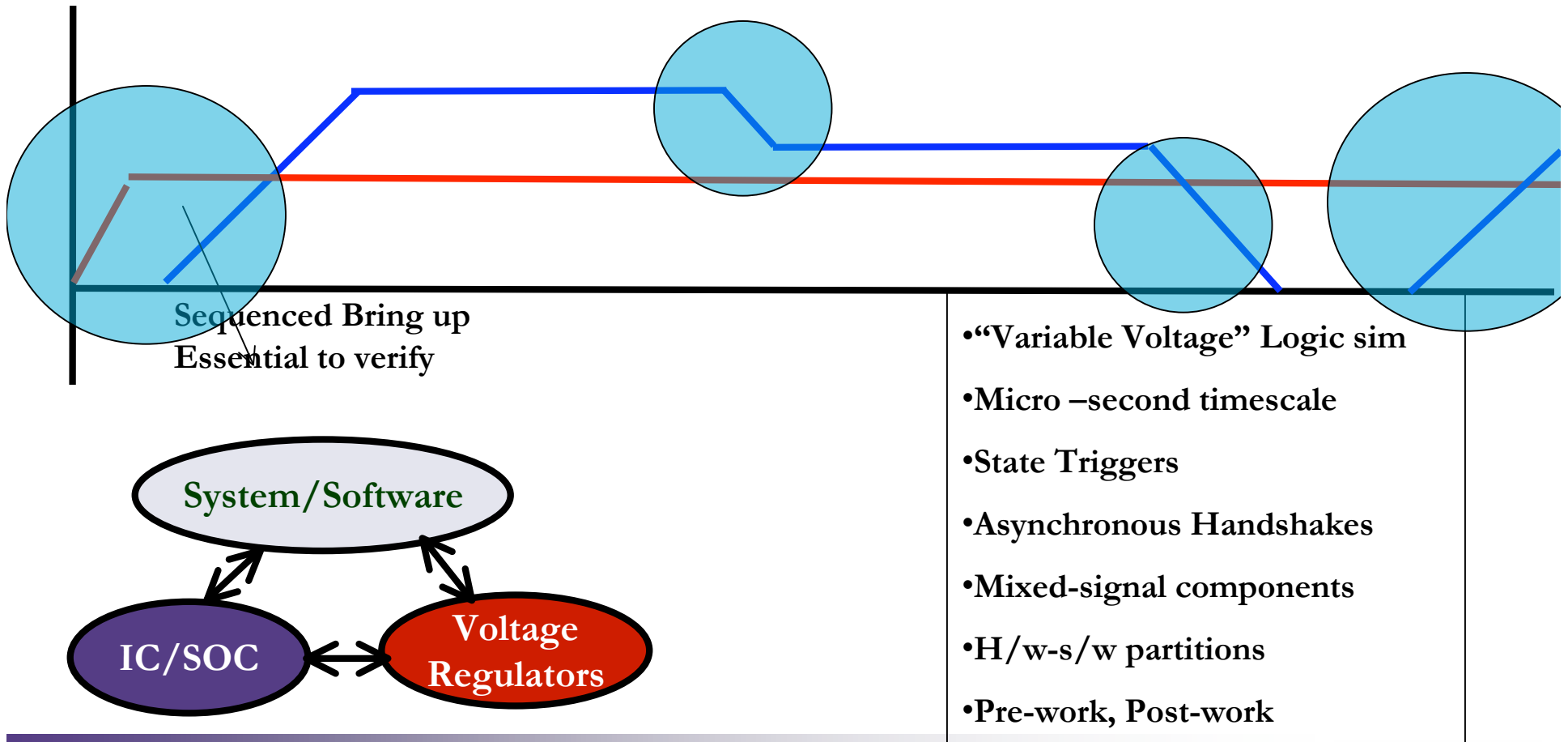
Voltage Aware Boolean Analysis (Electrical Accuracy)

Hybrid (Static-Dynamic) approach to conquer complexity

# Traditional Logic Verification

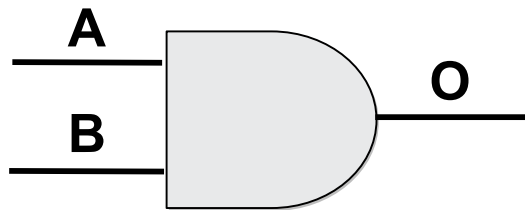


# Power Management Verification



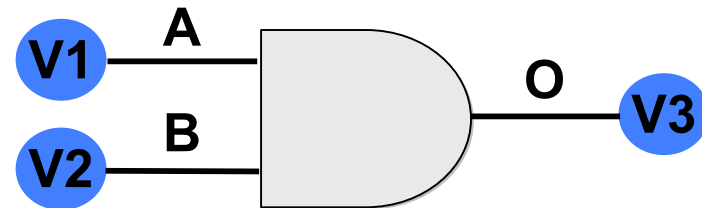
# Fundamental Technology Shift Enables Verification of Power Management

Traditional Boolean Analysis



A	B	O
0	0	0
...	...	...
1	1	1

Voltage-aware Boolean Analysis



V1	V2	V3	A	B	O
			0	0	0
			...	...	...
			...	...	...
			1	1	1

**Don't confuse this for X-injection!**

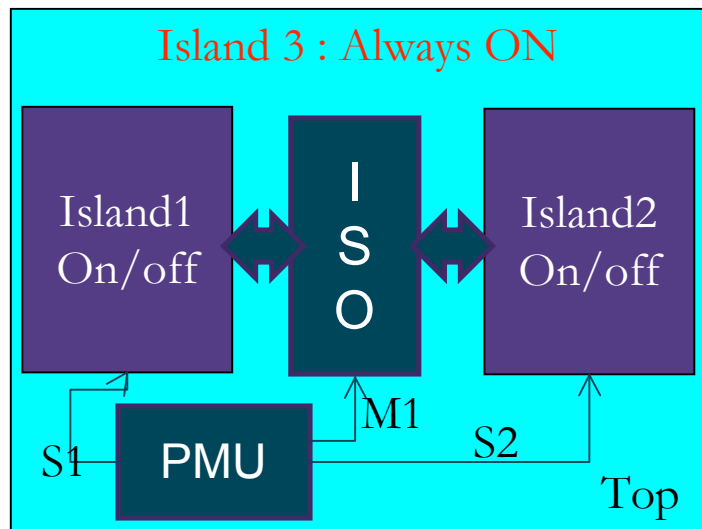
# Why is X-Injection Not Enough?

- Treats voltage as a binary value
  - No Voltage input into boolean equations
- X-Injection can't detect
  - Logic Conversion Errors
  - Power-on Reset Bugs
  - Voltage Scheduling Errors
  - Unplanned States, Unsafe States
  - Memory Corruption Issues
  - Power Gating Collapse
  - Multi-Fanout Issues
  - Voltage Sensing Handshake issues
  - Aborted Transitions

**We need all this and a sophisticated verification methodology**

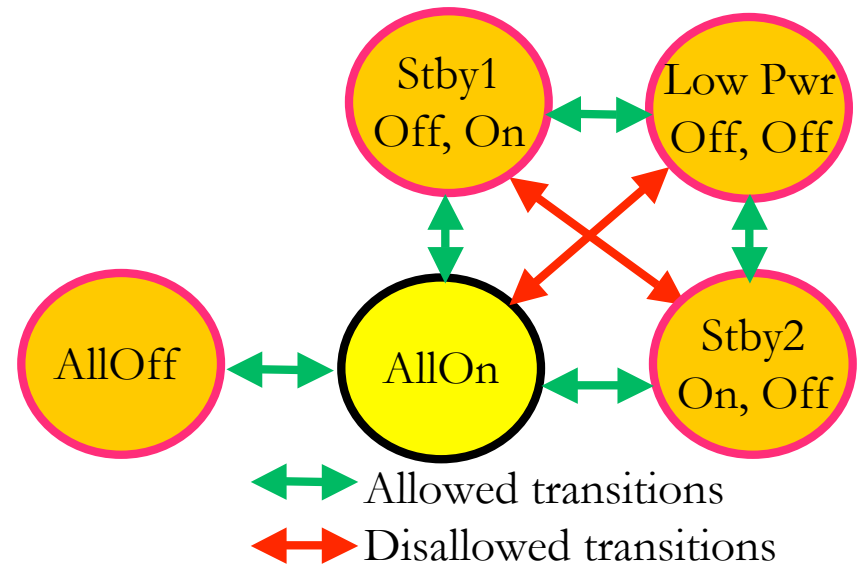
# Power Management Increases Verification Complexity

## Design



- Verification must ensure correctness of
  - Voltage Isolation Cells

## Verification

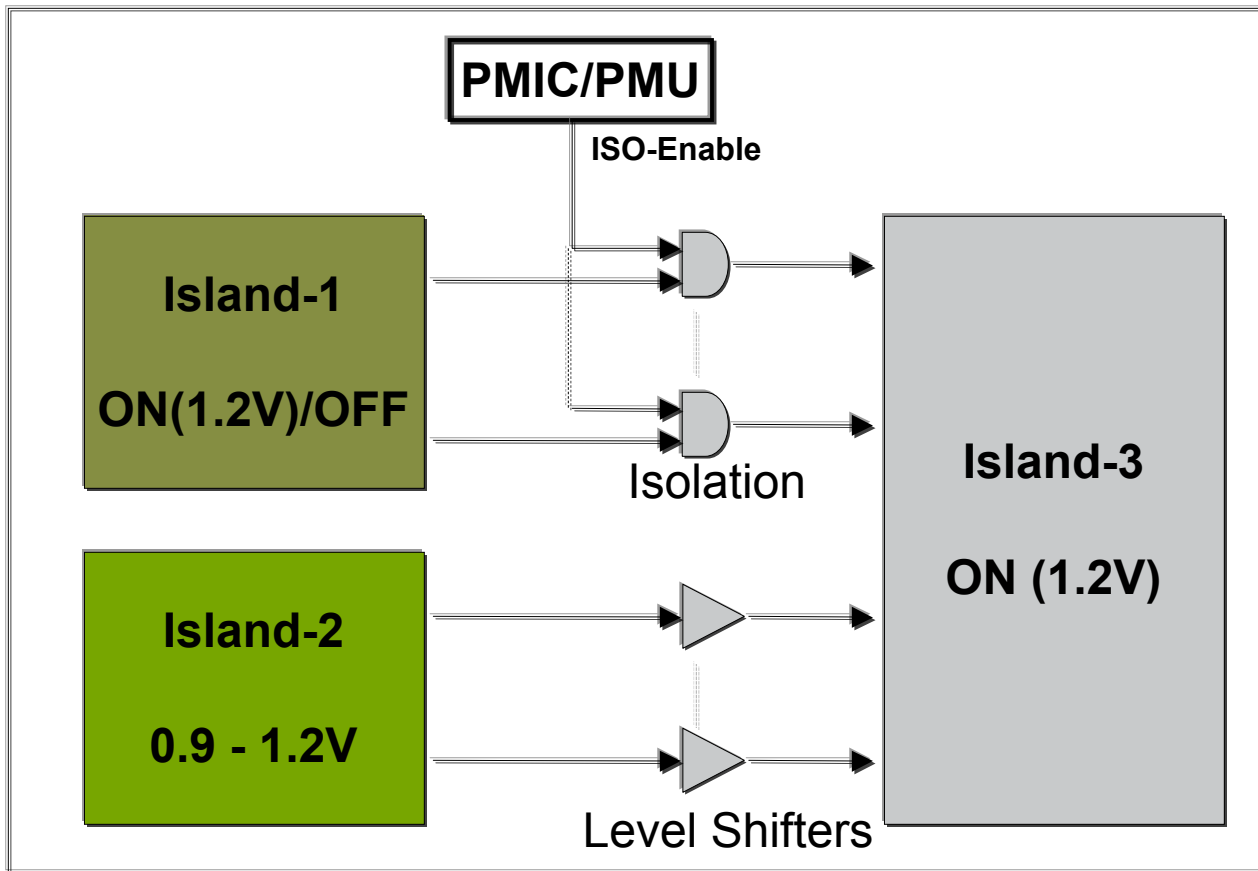


- Verification must be aware of
  - Power States
  - Voltage Transitions
  - Valid Power Sequences

# Traditional Coverage vs. MV Coverage

- Traditional : Directed and Random tests
  - Line, Toggle, FSM, Assertion Coverage
- Multi-Voltage
  - Static Coverage
    - Check isolation cells, level shifters etc.
  - Focused Dynamic coverage in each Power State
    - E.g. No need to cover isolated signals in On block
      - But need to prohibit toggles on off block inputs
  - Dynamic Coverage of Power State Transitions
    - A transition may be caused by more than one activation path
      - E.g. Laptop hibernates because  
Low Battery, Lid close, Inactivity
  - New Assertions to include Voltages, PMU components
    - What are these and how do you write them?
- Can we shift more items from Dynamic to Static?
  - Arch/uArch Analysis, Power Sequence analysis yield a lot of bugs!

# Structural Checks - Static

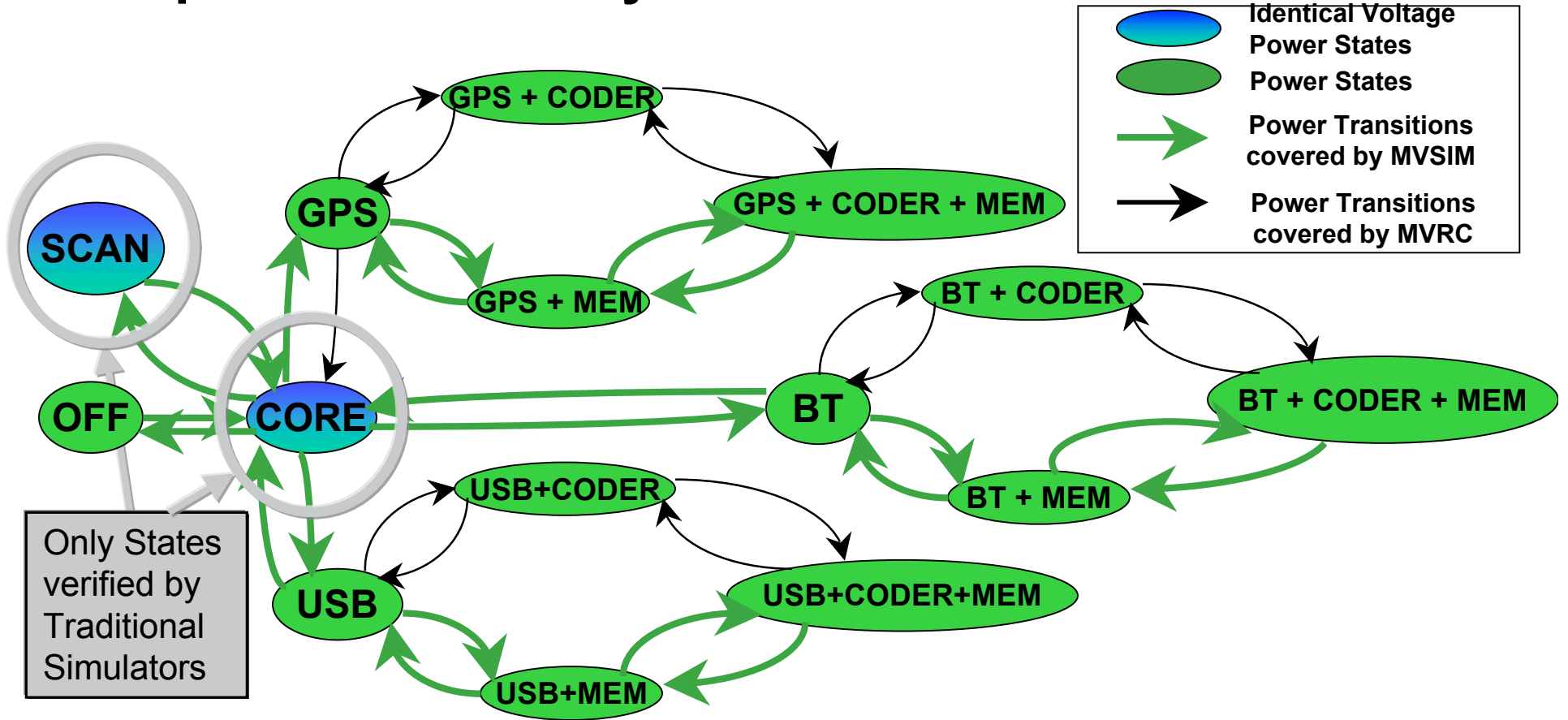


## Protection Cells

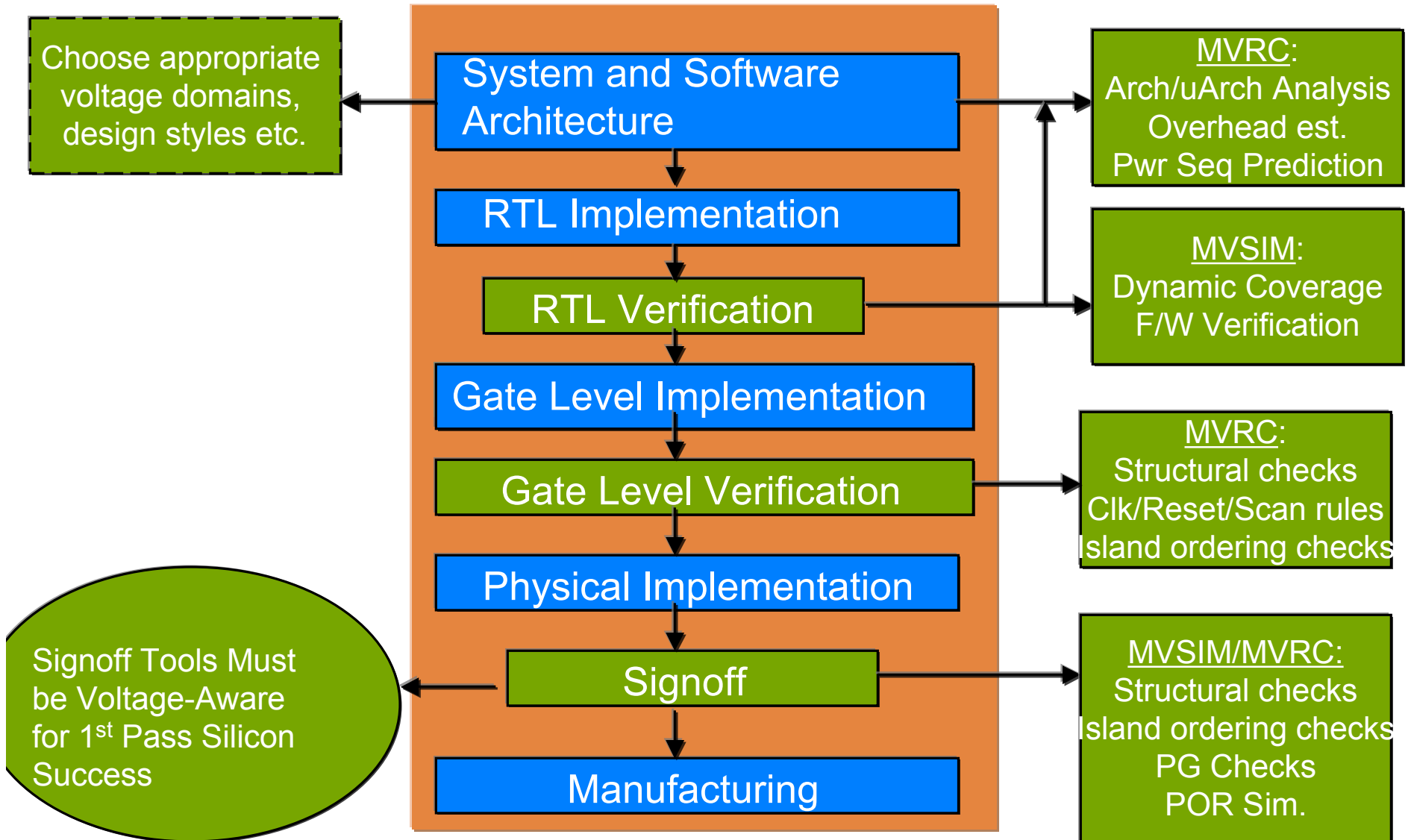
- Missing
- Redundant
- Incorrect type
- Incorrect island
- Isolation polarity
- Incorrect ISO-Enable
- Validates ISO-Enable network
- ISO-Enable polarity

.....

# Temporal checks – Dynamic and Static



# Power-Aware Verification Flow



# First-Pass Silicon Success With Synopsys (ArchPro)

ArchPro's comprehensive power management EDA suite offers an effective method to **reduce costs and time associated with the design cycles of low-power IC verification** and implementation. The tool provides an elegant solution to power management."

Michael Hurlston  
VP and GM, WLAN BU



"EDA tools for dynamic voltage scaling have only recently emerged. **ArchPro enables customers to verify their multi-voltage designs early, in the RTL design cycle**, thus reducing the risk of non-functional silicon."

Kevin McIntyre  
IEM Product Manager



"**ArchPro solutions not only verified our power scheme at RTL level, but also helped us debug some complex problems after the netlist** was generated. They really helped us get to the **sign-off**. We are pleased with their performance and the seamless integration with our flow."

Yoshio Inoue  
Chief Engineer, DFM & Digital EDA



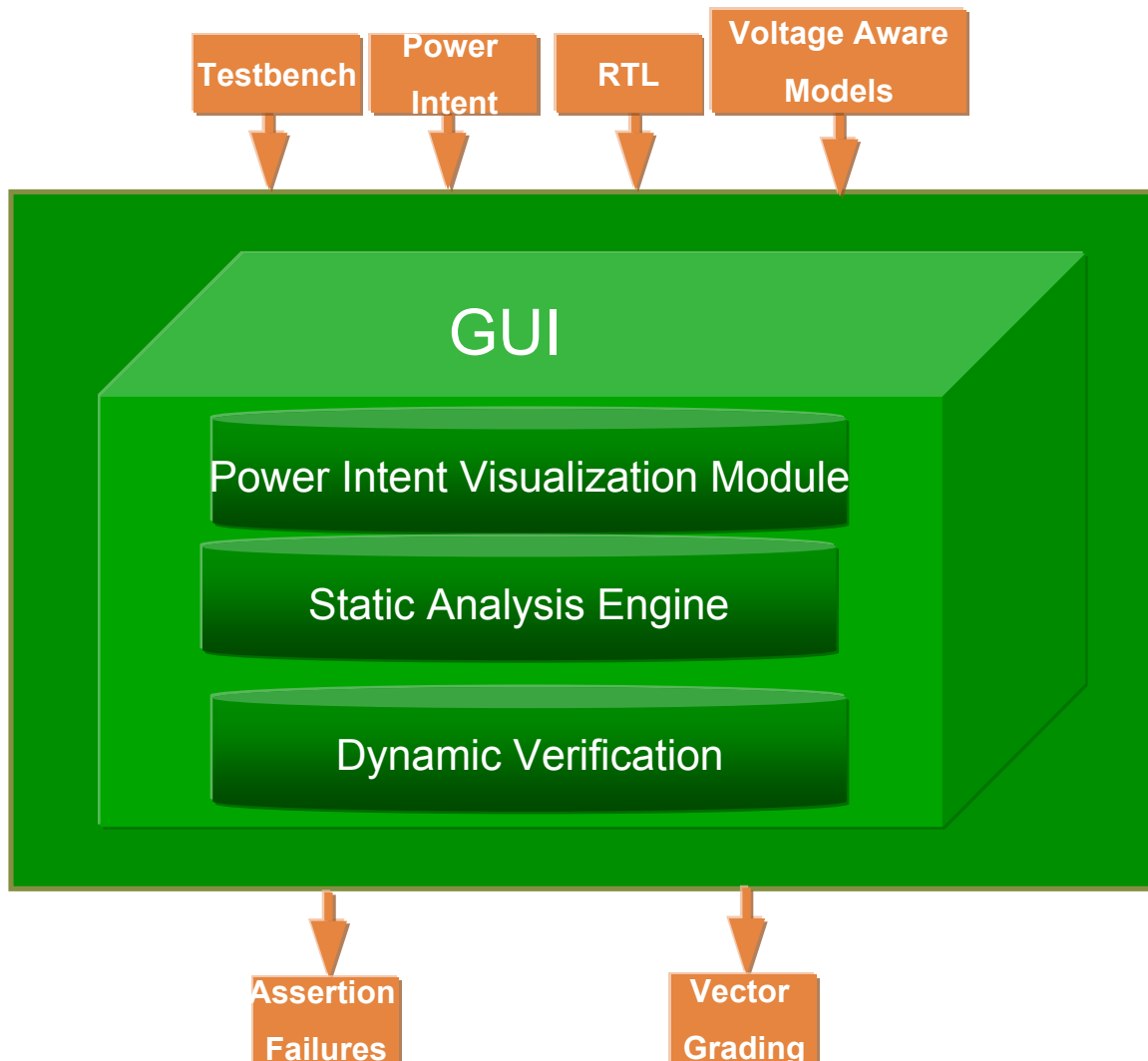
"... to maximize functionality while minimizing power usage. Working with **ArchPro is definitely giving us an edge in designing the next generation of complex, multi-voltage SoCs**, something we haven't seen anywhere else in EDA."

Mohammad Moradi  
Founder, CTO



**30+ design tape outs over last two years**

# Next Generation Verification System for Power Management



- Automatic creation of verification plan
  - Profiling of design and power intent and automatic assertion + coverage point creation
- Extended MV-Logical Analysis
  - All combinations of voltage and functional states supported
- Recommended Wake-up and Sleep sequences
  - Based on design and power intent

# Conclusion

- A 2X reduction in Dynamic Power and 10x reduction in leakage can be achieved
- Power Management always involves both hardware and software working together – esp. in mobile systems with ARM CPUs
- Verification of Power Management schemes is tricky and escapes traditional boolean analysis
- An effective verification strategy utilizes both static and dynamic techniques working together

# Thank you!

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